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PLATED-WIRE MEMORY STATE-OF-THE-ART STUDY (1972)

John M. Ives
Capt USAF

TECHNICAL REPORT NO. AFWL-TR-73-115

June 1973

AIR FORCE WEAPONS LABORATORY
Air Force Systems Command
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FOREWORD

This research was performed under Program Element 62601F, Project 88090327.

Inclusive dates of research were 1 October through 30 November 1972. The report was submitted 1 May 1973 by the Air Force Weapons Laboratory Project Officer, Captain John M. Ives (ELT).

Verbal briefings by Messrs. V. E. Cristensen, G. L. Grundy, J. A. Howe, T. E. Peckhan, J. A. Kolling, W. Gastafson, and R. Shimek of UNIVAC Division of Sperry-Rand, Inc., Minneapolis, Minnesota, and Thomas E. Anspach and Lawrence L. Norman of Honeywell, Inc., Aerospace Division, St. Petersburg, Florida, were found to be very helpful in coordinating information and bringing me up to date on the plated wire state of the art.

This technical report has been reviewed and is approved.

JOHN M. IVES
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ABSTRACT

(Distribution Limitation Statement B)

A wire plated with a magnetic surface can be used as a computer memory element by alternating the polarity of the magnetic field. While the wire in different enclosure configurations can hold its field in either a longitudinal or a radial direction, the radially oriented field currently is found to have many advantages with respect to switching speed, radiation hardness, and associated peripheral equipment. The construction of the wire presents many parameter balancing problems and needs very tight environmental controls for practical production. These problems have not yet been eliminated, keeping the bit cost in these memories high. The performance, however, of the radially oriented type compared to ferrite cores and semiconductor memories augments this high cost. A recently developed 2-mil wire size element eliminates some of the problems found in the previously standard 5-mil wire systems.

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SECTION I

MEMORY BACKGROUND

Technological advances in computer systems present a continuing demand for more efficient memory elements. Better switching speeds and larger storage memory cores are being called for by the civilian community; physically smaller cores, and cores hardened to shock, vibration, and radiation hazards are required by the government. Ferrite cores cannot meet all these demands; therefore, much research and development are being done to develop alternative forms of computer memories. Leading contenders in the contest to replace the time-proven ferrite cores are semiconductor memories, magnetic film memories, and plated-wire memories. All of these memories operate in a bistable mode: that is, they have either two stable steady states or one operating state and one nonoperating state. The chosen state defines a binary 1 or 0. The differences fall in the storage mechanism.

A ferrite core is a magnetic toroid partially encircled by an electrical conductor. The toroid generally has a nearly square I-ϕ hysteresis characteristic of the form shown in figure 1. A sufficiently large conductor current (greater than I_{01} or less than I_{02}) induces a permanent magnetic field (circling clockwise or counterclockwise, depending on the current polarity, representing the 1 or 0) which remains until altered by a large opposite polarity current.

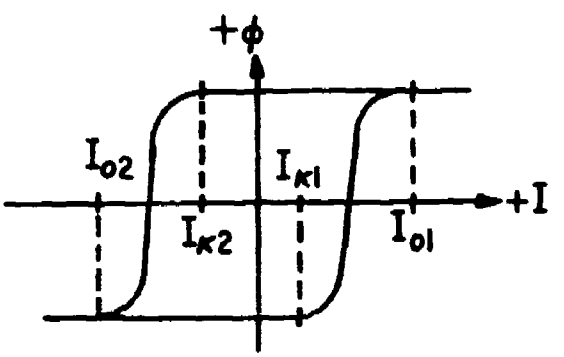

Figure 1. Sample Toroid Hysteresis Loop

Semiconductor memory elements do not use magnetic field storage, but rather electrical fields. One typical such element is a metal nitride oxide semiconductor (MNOS). This has a double insulator isolating a controlling gate from a P-N substrate. If the insulators are stacked vertically below the gate, the upper, a nitrate, insulator has the capacity to store holes or electrons. When holes are stored here, current in a P-type metal oxide semiconductor (PMOS) device is prevented from channeling between source and drain. If electrons are stored then the current flows. Naturally, changing gate voltage polarity determines whether the stored quantity is holes or electrons. The ability of current to flow or not flow represents 1 or 0.

The plated-film memory element consists of a thin Permalloy (80 parts Ni:20 parts Fe) magnetic film deposited on a nonmagnetic, insulator substrate. After the deposition, Permalloy exhibits an easy axis of magnetization: a preferred, although bipolar, direction that readily accepts and holds a magnetic field. Two electrical wires are then laid across the magnetic plane. One is a selection wire parallel to the easy axis, and the second is a sense wire perpendicular to it. A current pulse in the selection wire induces a field vector on the Permalloy film perpendicular to the easy axis field to give a declination away from the easy state. Upon release of this signal, the magnetization vector returns to the original more-stable mode. The returning magnetic field induces a current in the sense wire, the direction of which is monitored as a binary 1 or 0.

Plated-wire elements are an outgrowth of plated-film memory principles. U. Gianola of Bell Telephone Laboratories proposed in 1958 to use conducting magnetic wires with preferential direction of easy magnetization for use in computer memories. A solid wire, as he proposed, does not exhibit a uniform switching field at all radii and, thereby, makes switching speeds very slow. This idea, however, was refined by G. Hoffman and R. Turner of Great Britain in 1963, who patented the idea of coating a copper electrical wire conductor with magnetic material and then wrapping the coated wire with another conductor, analogous to the plated film's sense wire, that passes around the cylinder in a circumferential direction. From this point on the plated wire concept grew. The biggest step came in the sophisticated electrodeposition of magnetic film onto conducting wires in which the easy direction of the magnetic film was oriented circumferential to the wire. This can be done by applying a current along the axis of the wire while the electrodeposition is taking place.

Although main development of the new technology took place in the United States, commercial production of the element started in Japan by Toko, Inc. and Nippon Electric Co. and in France by Bull-GE. UNIVAC started the bandwagon in this country.

Like other memory elements, plated-wire elements are able to be organized in two-dimensional (2D), two-and-one-half-dimensional (2-1/2D) and three-dimensional (3D) arrays. Itemizing the differences between the different configurations at this point would detract from the brevity of this orientation section. However, the differences are important for evaluating operation of the memory. So, for the reader not familiar with these terms, an exposition can be found in the appendix.

It should be noted at this point that National Cash Register Company (NCR) Century Series computers are advertised as using plated-wire "rods" for their memory. The reader should not confuse this memory with the plated-wire memories to be discussed in this report. It is formed and works under a different technology. The rod memory element consists of an isotropic (no-preferred direction of magnetization) 98:2 Fe-Ni coating plated on a 10-mil BeCu conductor. The rod is wound with a continuous helix sense coil and separated word coils as illustrated in figure 2.

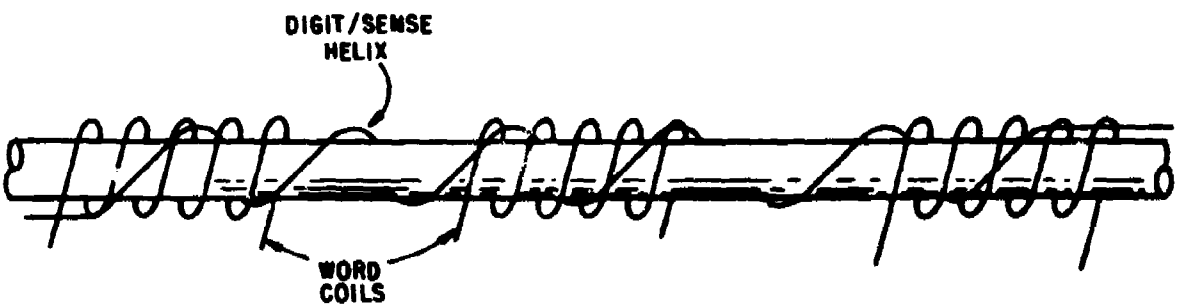

Figure 2. Plated-Wire Rod Configuration

An open-ended magnetization field is induced parallel to the axis of the wire by the direction of the current in the word coils. These define 0's and 1's which can be addressed by the sense helix as needed.

This is in strong contrast to the plated-wire element that is "anisotropic" and to be discussed in this report. This memory has its closed magnetic field circumferential to the axis of the wire as seen in figure 3.

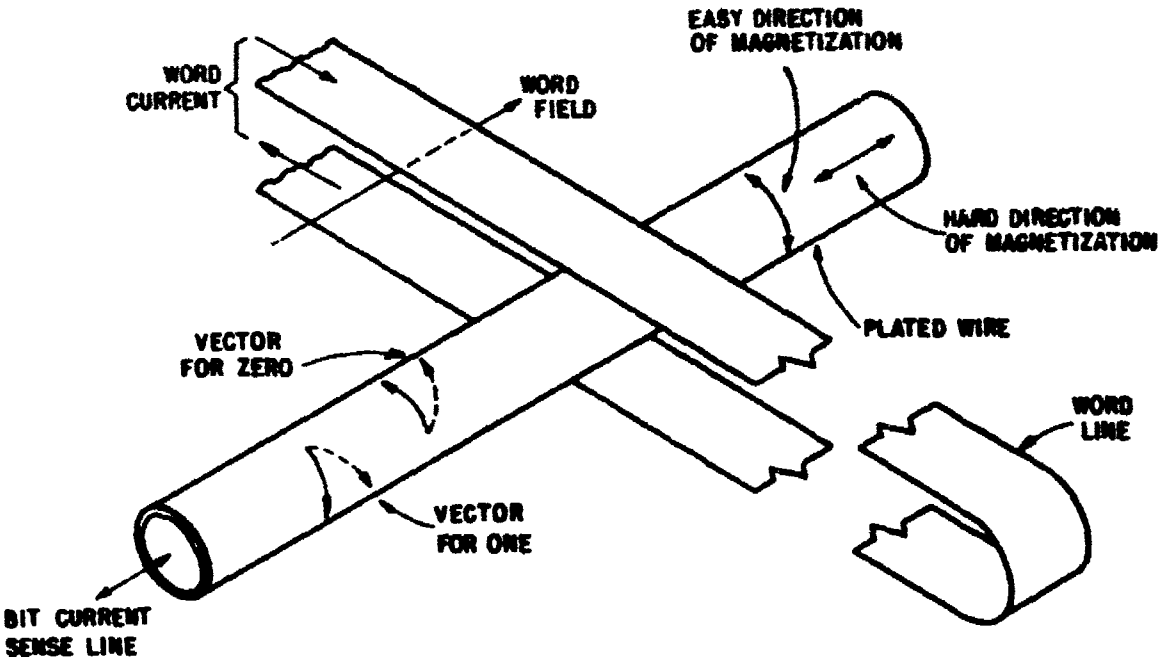

Figure 3. Plated-Wire Element

When the word current in the anisotropic memory is pulsed, an induced magnetic field vector is generated in the wire perpendicular to the established field that skews the resultant 1 or 0 impressed on the plated wire away from its easy state. The field returns to the original mode when the external force is removed, thereby self-inducing a current along the bit current axis whose polarity can be detected as being representative of the 1 or 0. If the word current is not so excessive as to destroy the impressed magnetic torque that holds the 1 or 0 field, the plated-wire memory can be operated under a non-destructive readout (NDRO) capability--a capability not available with ferrite cores--and, in general, a capability that can reduce the amount and, thereby, the cost of peripheral electronic circuitry.

The NCR rod memories are worthy of further study, but, as said before, this is a topic of a different technology and will not be considered further.

The plated-wire elements we will consider are not new to government systems. They are operational in Poseidon, Saturn, Minuteman II systems, and several NASA satellites. So, whenever examples are necessary for explanation, this paper will turn to those "real" systems to pick the necessary data.

SECTION II

CONSTRUCTION OF PLATED-WIRE ELEMENTS

The main blocking point for plated-wire memory (PWM) marketing seems to be the high cost, which is greater than $0.05 per bit for commercial uses, and greater than $0.10 per bit to meet government specifications. Technically, however, the plated wire compares favorably in most respects to, and many times exceeds, the features of other memories. High speed, bit capacity, and bit density are features to be praised in this memory. The bit density is limited mainly by the size of the crossing "word strap" wire. Currently, this is about 20 bits per inch. The plated wire itself doubles as a sense winding.

The basic schematic for the plated-wire concept was presented in figure 3. A 5-mil BeCu wire is thinly coated with copper which, in turn, has a 5000 to 10,000 Å layer of Permalloy film cylindrically deposited upon it. This is all done in a continuous electroplating process. Concurrently with the plating, a continuous direct current is run through the sense wire to align the anistropic magnetic material. This forces the easy axis to encircle the wire rather than run its length. The thickness of 10,000 Å is effectively surprising to those who have thought of anisitropy as a property of only thin film material. The anistropic properties work because the circular geometry maintains a closed loop of flux.

Microphotographs indicate that BeCu is a rough textured material that even under heat treatment retains randomly oriented substrate imperfections. These defects lead to bad electrical and magnetic characteristics. To correct this, before magnetic electroplating is performed, an electrodeposition of pure copper fills in these minor surface imperfections.

Ideally, the plated wire should be encircled with a conductive line "strap," to give a complete solenoidal effect in carrying the word current for read and write triggering. The sensitivity of the plated-wire bit, however, is not so dull that a full wrap is needed. General configuration uses a conventional printed word line that falls tangential to only one or two sides of the wire element. Other configurations have been used that are somewhat more efficient, but they have deficiencies that will be presented later in the report.

Information is written on the wire by the coincidence of word current and steering-bit current through the plated wire. When the bit current flows in the "one" direction, the magnetization vector is steered so that on release of the bit and word currents the vector falls in the one rest position. When the bit current flows in the other direction the vector falls in the zero rest position (figure 4).

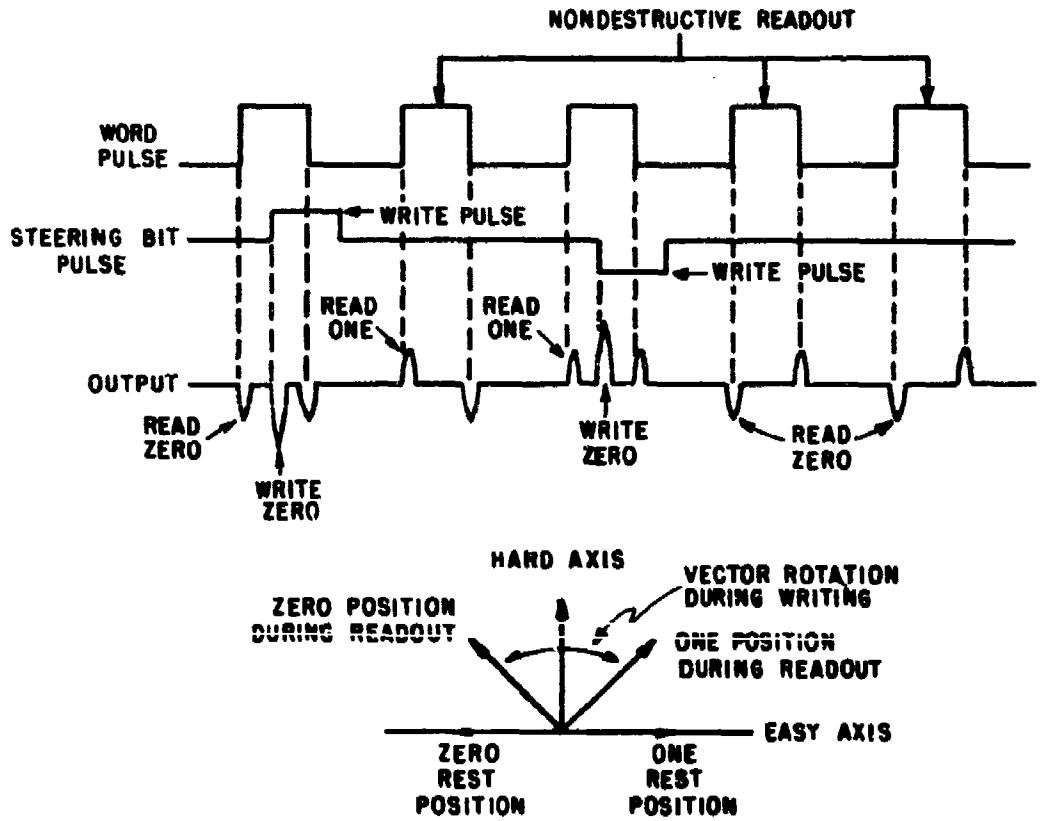

Figure 4. Simplified Plated-Wire Operating Pulse Sequence

To reiterate, each inch of wire generally stores about 20 bits. Since ideally the plated wire is magnetically invariant, the bit position is determined not by the magnetic configuration but by the positions of the word straps. A 5-mil plated wire generally has associated with it 40-mil word straps with 20-mil separations between them. This configuration is due more to production

convenience than to physical restraints. In its rest position, due to the closed flux path, an external field is essentially nonexistent; it is assumed, for practical purposes, to be contained within the material.

In production, plated wires are grouped with the word straps in two-dimensional configurations called "planes." These planes are stacked into arrays.

Construction of a plane is nearly all automated. A typical method used by UNIVAC is to put 8-mil piano wires covered with Teflon between two sheets of Kapton, which is a heat resistant form of Mylar. Glass epoxies with printed copper word straps are then placed above and below the Kapton-Teflon form. Setting this sandwich under high pressure and heat laminates the plane. The piano wires are placed under tension to decrease their diameter. When the piano wires are removed they leave cylindrical Teflon forms ready for manual insertion of plates wires. This technique is called the pulled wire tunnel assembly and is the one currently in use by the leading manufacturers.

A more efficient method has been experimentally developed and is expected to be used by UNIVAC in its 2-mil size plated-wire configuration. Instead of pulling holes in Kapton forms, 5-mil troughs are chemically etched in an epoxy. Then this etched configuration is sandwiched between Kapton-insulated copper word lines. It is anticipated with this method that automatic insertion of the plated wire may be attainable. As of yet, the manual method is still the safest and most reliable.

Another configuration used is the original one devised by Toko Coil of Japan for its licensee in the United States, General Precision's Librascope Group in Glendale, California. Here the word lines consist of insulated wire woven about plated bit lines as portrayed in figure 5. Unlike the manual insertion needed after the tunnel processes, a machine much like a textile loom weaves the strap wires back and force in programmed turns. Major advantages of this are a high production speed and the keeping of solder connections at a minimum.

The woven bit-line method has other technical advantages compared to the lamination method. Because the word wires wrap almost 180° around the plated wires instead of being tangent to them at only two points, there is a greater ability to shape the word fields more precisely; that is, they are strong and

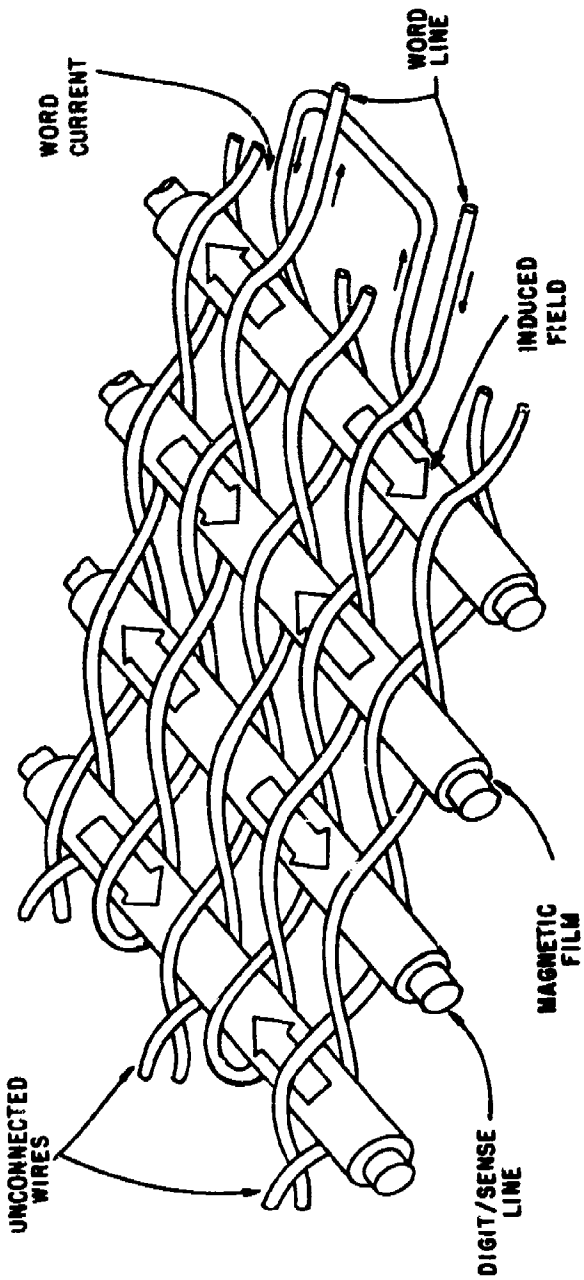

Figure 5. Woven Bit-Line Plane Configuration

uniform at the bit and fall off more rapidly away from the bit. In turn, the better coupling leads to better packaging density and allows the use of lower word current.

This configuration, however, is not nearly as mechanically stable to vibration and shock. Personnel at Honeywell, Inc. who concentrate on improving state-of-the-art packaging techniques say the idea is potentially valuable for high-volume production, and they hope to stabilize the structural weakness.

The memories are generally designed to cycle in the 500-nsec range. To achieve this speed, the plating process used must be tightly controlled. To produce a yield acceptability greater than 50 percent at least 24 variables must be monitored and flow rates must be tightly controlled. To meet basic specifications the wire must have (1) a high disturb threshold, (2) a zero magnetostriction composition, (3) an appropriate thickness of plating that gives a reasonable signal-to-noise ratio, (4) a thickness and compositional uniformity along the length and circumference of the wire, (5) as low a skew of the easy axis as possible, (6) a low value for the anisotropy field, H_k, and (7) a moderate value of dispersion.

Approaches used to try to solve some of these problems are discussed below. It is, of course, understood that optimization of one parameter might have to be done at the expense of others.

Plating a layer of copper between the BeCu substrate and the Permalloy layer serves other functions besides filling substrate surface defects. While gross defects in the original wire such as dye marks, inclusions of foreign material, and gouges must be avoided to eliminate bit failures, a controlled surface roughness is beneficial to provide the magnetic memory bit with a high disturb threshold--that is, a bit threshold not influenced by the writing of adjacent bits. To achieve this the copper density is deliberately controlled to produce a rough scalelike deposit. A maximum coercive force exists for a particular amplitude and frequency of the scalelike surface for a constant thickness Permalloy film. The Russian physicist, Lesnik (ref. 1), predicted that the coercive force is dependent on the amplitude and periodic roughness of the

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Ref. 1. Lesnik, A. G. et al., "The Influence of Roughness of the Substrate on the Coercive Force of Permalloy Films," IZV. Akad. Nauk SSSR, Vol. 29, pp. 594-598, 1965.

magnetic film, as well as the roughness of the substrate. However, his model is based upon the assumption that the substrate is wavelike and has a sinusoidal form which is not true for the roughened copper underlayer. But this theory is extended loosely in a generalized sense to the point that the total magnetic energy of a wall, if the wall width is less than the surface wavelength, depends on the number of modular growths through which it passes.

Two other techniques have also been proposed to provide a high coercive force element: the deposition on a smooth substrate the ternary Ni-Fe-Cu alloy as the magnetic film, and diffusion of Sn into the Permalloy film. No reports on the effectiveness of either of these techniques are available, so the use of the substrate-controlled roughness technique is the way the problem is being attacked today.

Since magnetostriction, the property whereby physical dimensions vary with the magnetic field, is a function of the magnetic layer crystallographic orientation, the controlled substrate roughness seems to minimize this problem, too. The plated-wire memory can be very sensitive to stress. To prevent failure due to stress and still give a 50-percent yield, the composition of the film must be held to less than 0.2 percent of the zero magnetostriction composition (ZMC). Again, this is done by putting a very tight tolerance of the electrolyte flow: a flow rate in the order of 1100 ± 150 cm^3/min.

Since a 5000-Å film is not considered thin film, problems present themselves in the plating process as deviations from the ideal. The standard potentials of nickel are -0.250 volt and that of iron -0.440 volt. Electrochemical theory predicts that Ni ions should be preferentially deposited. In practice, however, the iron ions deposit at a faster rate than the Ni ions, a process entitled "anomalous codeposition." To get the proper Permalloy composition in the anomalous codeposition process, the initial ion bath must be in the ratio of 50:1.

This violation of the electrochemical law is not well understood. One proposition is that ferrous hydroxide is formed in the solution and absorbed at the cathode suppressing the deposition of Ni, but permitting a high rate of iron discharge.

Another consideration in the plating process is that, since a nonthin film is deposited, an iron-rich composition gradient has a tendency to form. This is currently minimized by pulse plating, although agitation and programmed current variations are alternative methods.

Iron ions in the bath have a tendency to form iron oxide with the air which precipitates, causing the need for a continuing replenishment of the iron ions to keep the proper NiFe bath ratio. UNIVAC has solved this problem by plating in a nitrogen-argon atmosphere.

Variations in bath temperature change the rate of diffusion of metal ions into the depletion layer and, thereby, effect the composition of the deposited alloy. Therefore, to maintain the ZMC this temperature must be maintained to within $\pm$ 0.2°C. This is naturally difficult. A possibility exists in extending this temperature parameter by adding certain metal ions such as copper or cobalt to the metal bath. However, this is done at the expense of modifying the magnetic properties, notably increasing the anisotropy field, H_k.

The thickness of the magnetic deposit is a function of cathode efficiency, current density, and time. An efficiency of about 90 percent can be maintained by controlling the pH of the solution constant at a value of 3.0. This can be ensured by adding either boric or citric acid to the open-air bath. These acids provide the needed buffer and, likewise, form soluble complexes with ferric oxide which may otherwise precipitate on the plating coating.

These factors must all be taken into consideration before the plating is begun. Once the operation starts it must be kept working 24 hours per day, 7 days a week until sufficient production is attained. It is a major job to start the process. A new start to "tune" the plating process until satisfactory results are obtained takes anywhere from 8 to 24 hours; the balancing of parameters is more of an art than a defined technical procedure.

Wire plating is run at a linear feed of about 12 inches per minute for government wires and 18 inches per minute for standard commercial specifications. The wire is fed in a continuous stream from a large spool into the various plating baths, an annealing furnace, through an on-line tester, and a wire cutting machine (figure 6). In this feeding of the wire, mechanical problems must be solved. Twists in the wire during the magnetic plating operation will result in the development of a magnetic skew when the wire relaxes to the untwisted state. This skewing can be minimized by pushing the wire instead of pulling it through the system so that one end of the wire is free to twist and will not maintain a torsional strain.

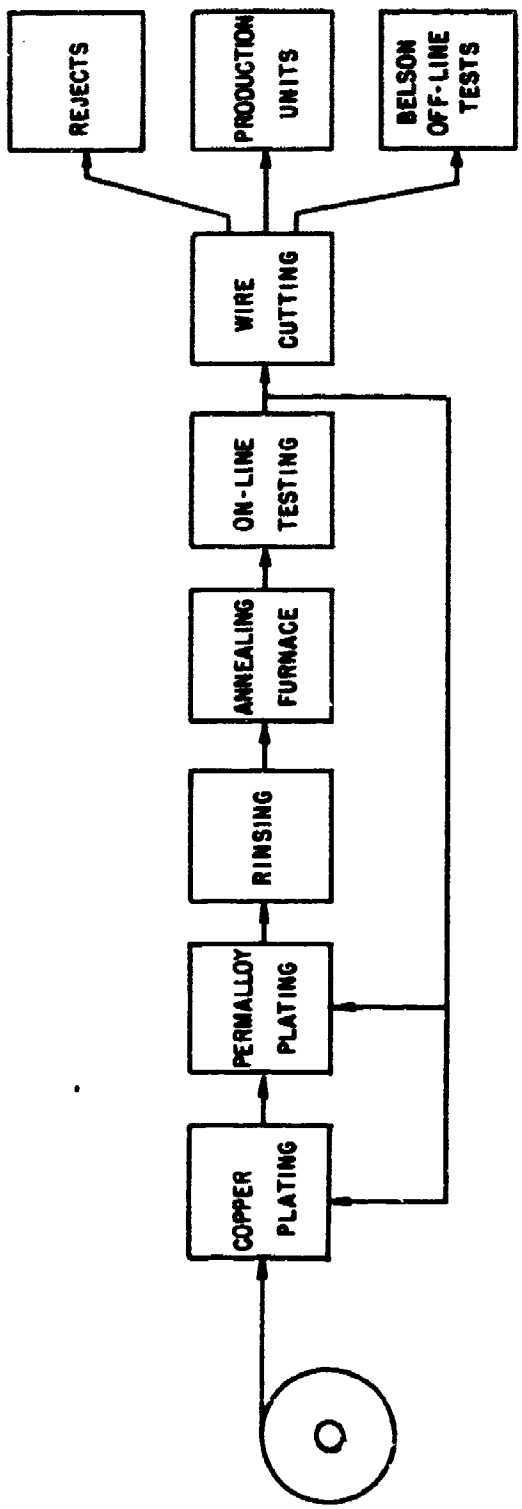


Figure 6. Plated-Wire Production Line Steps

The wire to be used should be of good quality, free from extrusion dye marks, inclusions of nonmetallic particles, and gouges. It has been found that a one-to-one correspondence exists between these defects and failure parameters after plating. A longitudinal scratch causes greater degradation than an equivalent circumferential scratch, so occasionally wires containing the latter may be deemed acceptable.

In the operation of the system during the plating cycle a current of 1 ampere is pulsed through the wire to produce a field of 32 Oe. This orients the magnetic domains circumferentially to produce the film with a skew of less than 20 mOe.

Long ago it was observed that plated wires began to change their magnetic characteristics immediately after plating--particularly if they are subject to word drive currents in a memory--in a process described as the "aging" of the wires. This aging is a result of the migration or annihilation of point defects produced during the electrodeposition process. The phenomenon can be retarded be eliminating or locking these defects immediately by annealing the plated wire. A temperature of 300 to 400°F for a period of 1 minute in a magnetic field of 30 Oe does a fine job of slowing the aging process down from an operational "lifetime" that previously was measured in months or years to one that is now counted in decades.

A lifetime definition has not been standardized, but Honeywell's definition can be used as a standard for purposes of this report. A lifetime of a memory is described as the time the output voltage of the memory reaches about 60 percent of the starting voltage, or the H_k has a skew of less than 45 degrees. Prediction of the lifetime comes from complex models for a newly formed wire, but they are all based on the Slonczewski kinetic equation.

$$\frac{dW_j}{dt} = \frac{1}{\tau_j}\left(W_{eqj} - W_j\right)$$

where

W_j is the energy associated with one component of the magnetic anisotropy

W_{eqj} is the equilibrium value of that energy

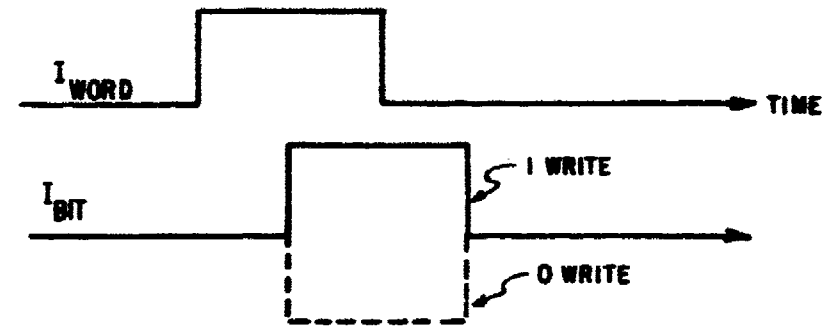
τ_j is the time constant with which the process proceeds

Academic objections have been made to this prediction model since it is based on assumptions that the various processes that occur during aging are reversible, they proceed independently, and that τ_j is a constant. Observations indicate that the first assumptions are not completely true and τ increases as time increases but when this formula is assumed as a worst case approximation it performs an excellent function.

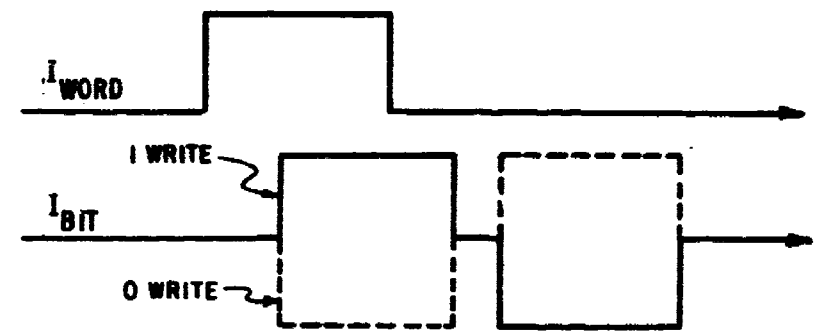
That testing can be made continuously on line is a great production advantage for manufacturers of plated-wire memories; however, the testing must be carefully planned so that it does not appreciably accentuate the cost involved by slowing production rate. At the same time the testing results should be fed back to modify the electrochemical deposition parameters as needed and be validly representative of the behavior of the wire in a memory stock. For this last reason a set of tests on the wire is generally designed for the configuration in which it will be used. Luckily, most parameters monitored are usually similar. For example, the fundamental magnetic properties are the anisotropy field, H_k, and the saturation magnetization, M_s; an example of system properties are output voltage, disturb threshold, read and write operating points. These parameters, among others, are always measured.

A minimum of eight test points should be monitored in production. "High" and "low" in the following discussion are to be taken in a sense relative to the design nominal values. Proper currents should be pulsed to give (1) an isolated high word field; (2) a stray bit field inside the designed creep limit; (3) a high-word, low-bit field; (4) a high-word, high-bit field that is within the adjacent word disturb limit; (5) a low-word, low-bit field that writes and provides minimum output voltage response; (6) a low-word, high-bit field that does not affect an adjacent word disturb; (7) a stray word, high-bit field that is inside the creep limits; and (8) an isolated high-bit field that is less than the hard axis field, H_w. These write and disturb field-point threshold parameters evaluate operation at random positions on the wire.

It should be noted that the relationship of word and bit current used for writing information in this testing is very important. The testing of the element must be relevant to the write sequence used in the memory system. For example, the adjacent word disturb (AWD) threshold for single-phase, bit-current write scheme as shown in figure 7a is grossly different from that of a two-phase scheme consisting of two sequential pulses of bit current of opposite polarity as illustrated in figure 7b.



a. One-Phase Write Pattern



b. Two-Phase Write Pattern

Figure 7. Common Word Bit-Line Write Patterns

This difference occurs because the second pulse reverses the creep of the first pulse and, in practice, is the usual way write sequences occur. There are, however, other more subtle differences in test write patterns such as word-per-bit-field time coincidence and pulsewidth sensitivity. The best approach includes first determining worse-case limit of operation parameters, then testing to these limits to provide a reasonable assurance of proper performance.

The testing of all options on all bits is virtually impossible, so compromises must be made. Bit lengths are determined by the word straps after completion of the memory unit, so precise locations prior to assembly are almost always unknown. Therefore, every bit length should be tested with partially overlapped sequences.

Wires are randomly sampled after proper completion of the on-line tests, to be also monitored for production quality in skew, dispersion, and creep. These are long-term tests and are measured using a standardized Belson test machine. In general about 10^6 to 10^8 pulses are written and read at bit lengths on the machine. Variations in the skew, dispersion, and creep are monitored, and if they do not meet defined specifications, complete lots of plated wires may at this point be rejected.

Other tests are also performed off-line to measure the following magnetostriction coefficients: K_E, tension magnetostriction; K_T, torsion magnetostriction; and K_D, nondestructive readout (NDRO) magnetostriction. In measuring K_E, a 50-gm load is hung from the plated wire. A half-nominal word current is impressed and the reduced value of H_k is measured. K_T is determined by twisting the 12-inch segment of wire $\pm$ 90 degrees, measuring the skew. If the skew angle, β, varies more than 0.5 degrees in this test, the composition is not within tolerable values for ZMC. K_T has experimentally been found to have a strong simple correlation to K_E and is more sensitive to composition departure from ZMC. Therefore, it is doubly used on-line as a backup ZMC test.

With the 50-gm load impressed after measuring K_T, a nominal word current is impressed on the wire, and the digit current is monitored. Comparing this value with the digit current measured without a load gives the coefficient K_D. This parameter is uncoordinated with either K_E or K_T and does not depend on H_k. This led to the premise that K_D is associated with the surface roughness, and, so far, this assumption seems valid. It is used, depending whether the value comes out positive or negative, to indicate, respectively, an increase in the minimum digit write current dispersion or as a destruction of the NDRO properties of the wire.

The Belson tests with the magnetostriction measurements are sometimes made over a typical 100°C (-30°C to 70°C) range of temperatures. Detailed variations of parameters with temperature can be found in papers listed in the bibliography. In general, however, over this temperature range the measured parameters have minimal variations, and almost all variations are linear or nearly linear making wide temperature range operation amenable to very simple design.

Radiation susceptibility of various magnetic memory elements is being studied by Gulf Radiation Technology. Components are being exposed to simulated radiation environments and in the Minute Steak underground nuclear shot. The data and the

results are classified SRD. The interested reader can find the details in technical report GULF-RT-A1160. In general, however, it can be said that while all magnetic elements are inherently hard to radiation, the plated-wire element proved superior in many respects.

At this point it should be pointed out that a closed set of design equations does not exist to permit a straight analytic design of plated-wire memory planes. The magnetization distribution in the element, the domain wall structure, the drive-field dynamics, and the sense line interactions are so complex that only approximate analytic solutions, derived from highly simplified models, are available. Of course, if space is not a limiting factor, then interactions can be minimized; but, almost always, memory specifications call for packing as much memory into as small a space as possible. A typical high-bit density is one in which the word straps are separated by 0.040-inch centers along wires separated by 0.015-inch centers to give a 1667 bits/in^2 maximum plane density. For such memories a magnetic "keeper," a material of low permeability that is placed around the bit position to concentrate the flux lines and minimize stray flux fields, must be added to the element configuration. But even the "keeper" does not solve all the magnetic problems. Magnetization ripple; the roughness of surface topography; domain-wall locking and mobility; magnetization creep; variations in both magnitude and anistropy from site to site; the failure of thick high-dispersion films to follow the models used in general magnetic film theories; and variations in H_c, the coercive force; H_v, the domain-wall motion threshold; and H_o, the creep threshold from site to site are only some of the more important restrictive criteria that limit the usefulness of current magnetic calculations. The engineering world has much mathematical and theoretical work yet to do before plated-wire plane design can graduate from the art to the engineering state.

Two basic forms of PWM plames are in use today: the half-turn memory plane and the full or multiple-turn magnetic plane. These are illustrated in figures 8, 9, and 10.

The half-turn configuration has all the word straps connected to a ground plane located closely to the plated wires. This is a particularly simple form of construction since no alignment is necessary for a word line return or for

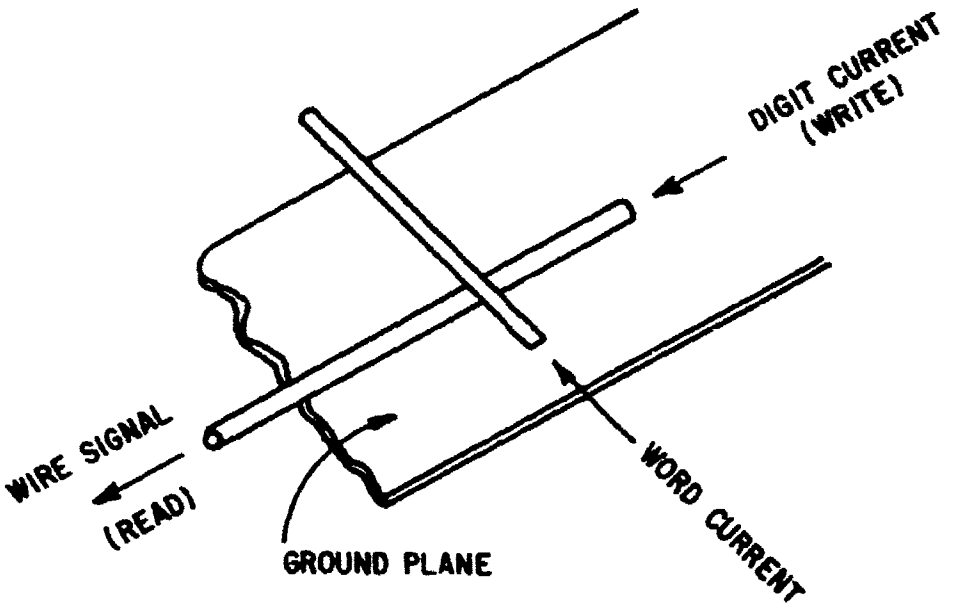


Figure 8. Half-Turn Word Strap Configuration

alignment of the plates wires; it, also, exhibits a desirable low impedance in the 50-ohm range. However, on the other hand, the common ground causes many problems of crosstalk and eddy current fields.

In writing, digit current flowing in a selected wire induces crosstalk signals in the wire's neighbors which can detract seriously from operating margins. Also, during readout, crosstalk signals from adjacent wires can significantly modify the readout amplitude of the selected wire.

As much as 40 percent of the total applied drive field can be derived from eddy currents in the ground plane. The decay of these eddy currents causes the applied field at the end of the drive pulse to be lower than that at the start. Further, the eddy currents induced by the falling edge of the drive current generates an opposing drive field that can substantially reduce the applied field of the next word pulse. For short pulses, 100 to 200 nsec, with a duty factor of 60 to 75 percent, the last pulse of a long sequence of equal current amplitude may only generate a field of 75 percent the field of the first pulse in the sequence. However, good keeper design is able to reduce this loss of field amplitude to a few percent.

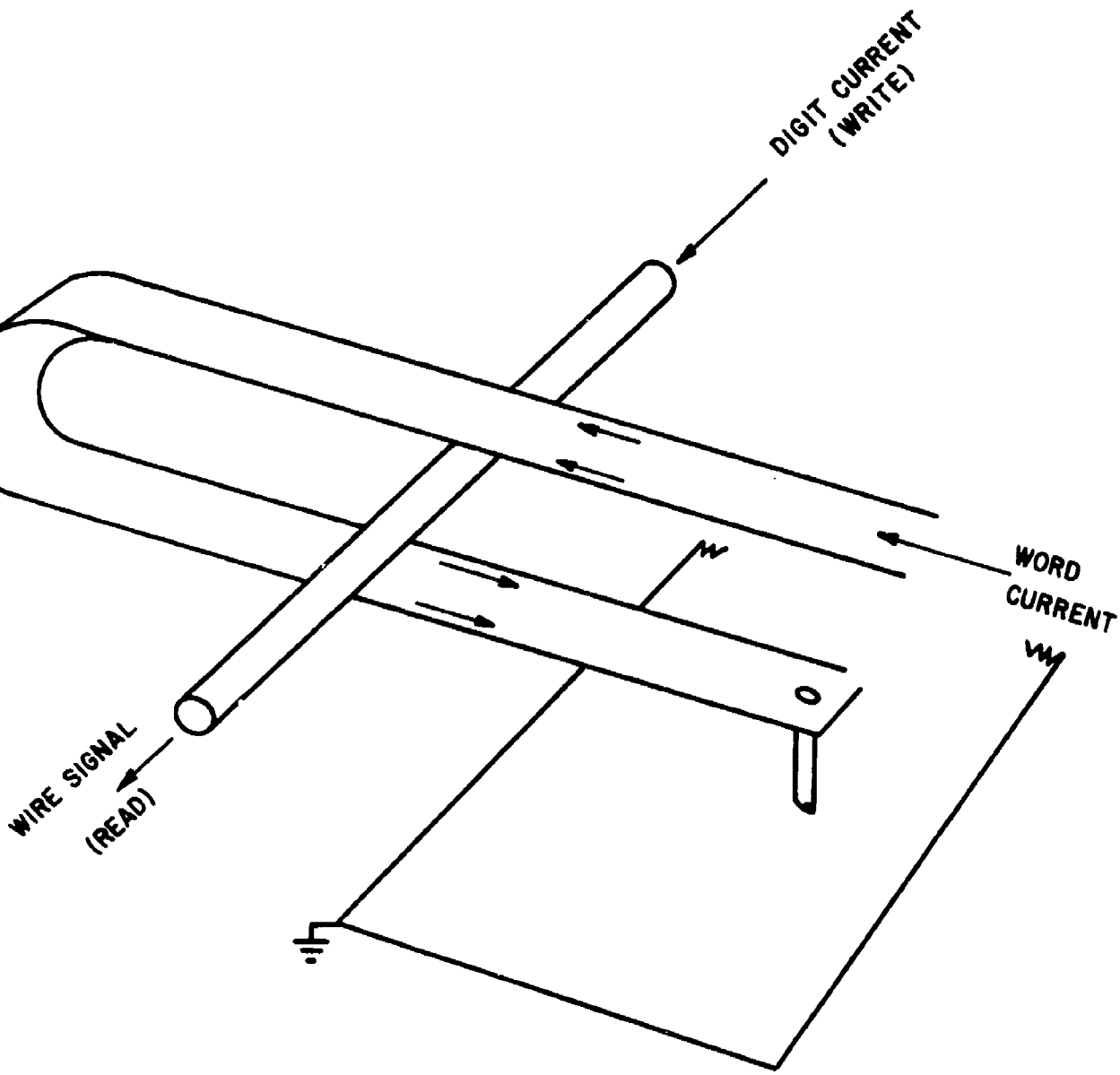


Figure 9. Full-Turn Word Strap Configuration

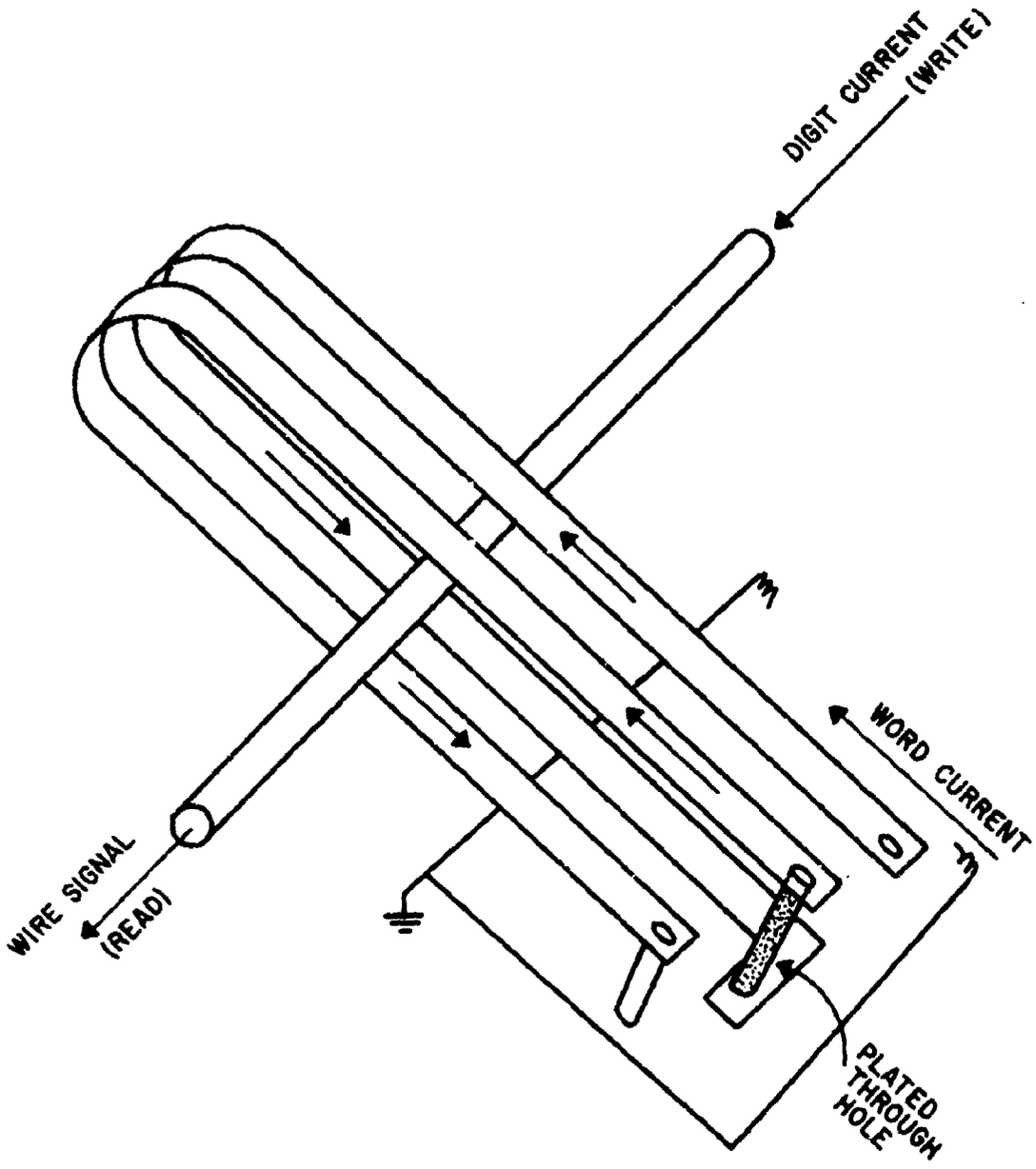


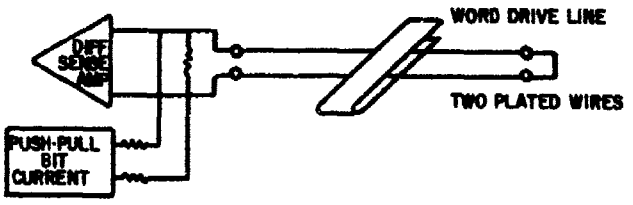
Figure 10. Two-Turn Word Strap Configuration

The more commonly used plane configuration is the one or two full-turn drive strap configuration. It too experiences field variations, but in a different manner. If the ground plane is 25 mils or closer to the word line, the applied field at the start of a drive pulse is smaller than at the end of a pulse because the field from the ground eddy currents opposes the drive field. Similarly, the induced eddy currents at the end of the drive pulse also generate an aiding field so that the field of the second pulse will be larger than the first even though both were of equal drive current amplitude.

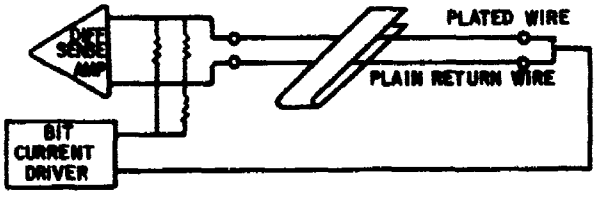
The principal advantages of a full-turn, drive-line construction is the lesser eddy current effect on applied field because the ground plane is further away. Comparing nonkeepered configuration, this latter construction provides 25 percent more Oe/Amp of drive current. The price for these advantages is the alinement of top-to-bottom word lines, poorer sense-line characteristics, and more assembly steps.

A good improvement on the above full-turn drive line is to remove the ground plane from close proximity to the drive word lines. This eliminates most of the pulse width and duty factor sensitivity. Also, while the adjacent word lines themselves can cause variations of several percent because of eddy currents induced in them, slits in the word line, thinner copper, or a material of higher resistivity copper alloy can reduce this effect to negligible proportions. When this is done one more factor must be considered. Without the ground plane, it is necessary to use a return wire for each plated wire to form a balanced transmission-line pair. This is done by using another plated wire or a plain wire return. We can use two-strap, bit-line intersections to define a single memory bit which provides a signal of twice the amplitude. Figure 11a shows a simplified form of the hookup. However, the bit-write transient formed is a serious disadvantage in this configuration; it presents a large differential signal that can overload the differential sense amp. Figure 11b provides the first order cancellation of the bit-write transient, but since it uses a plain wire in the place of the original plated wire it gives only one unit of output signal. But, the changing of wires is necessary. If this were not done the stored information would be the same polarity at each input to the diff amp cancelling the desired signal.

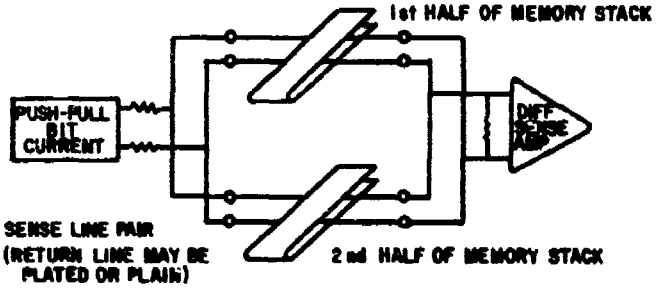
In general, however, for good reliability the bridge network shown in figure 11c is the most common setup used. It provides cancellation of the bit-write transients and achieves the doubled signal wanted if both bit wires are plated.



a. A Two-Strap, Single-Bit Line, Plated Wire Return



b. A Single-Bit Sense-Digit Line, Dummy Wire Return



c. Bridge Configuration

Figure 11. Three Sense-Digit Line Configurations

The strong disadvantage is that the doubled wire count, as compared to the other configuration, results in a loss in packing density, and the sense line characteristic impedance is increased 30 to 40 percent.

The double plated wire used as above is most often a single wire bent into a hairpin structure. While this operation, as compared to other steps in the plated-wire manufacture, seems so comparatively simple, it is one of the most critical operations performed. Wires with zero magnetostriction for torsion, tension, and bending on a selected axis perpendicular to the wire axis can still be relatively sensitive due to circumferential variation due to plating cell

geometry and flow conditions that have not yet been defined. A kink in the hairpin bend visible at 450X magnification is enough to impede current flow, and at Honeywell has accounted for as much as a one wire in four reject. UNIVAC, however, has patented a printed circuit hairpin which they claim solves this rejection problem; it supposedly generates no impeding fields. A sketch of the structure supplied by UNIVAC can be seen in figure 12.

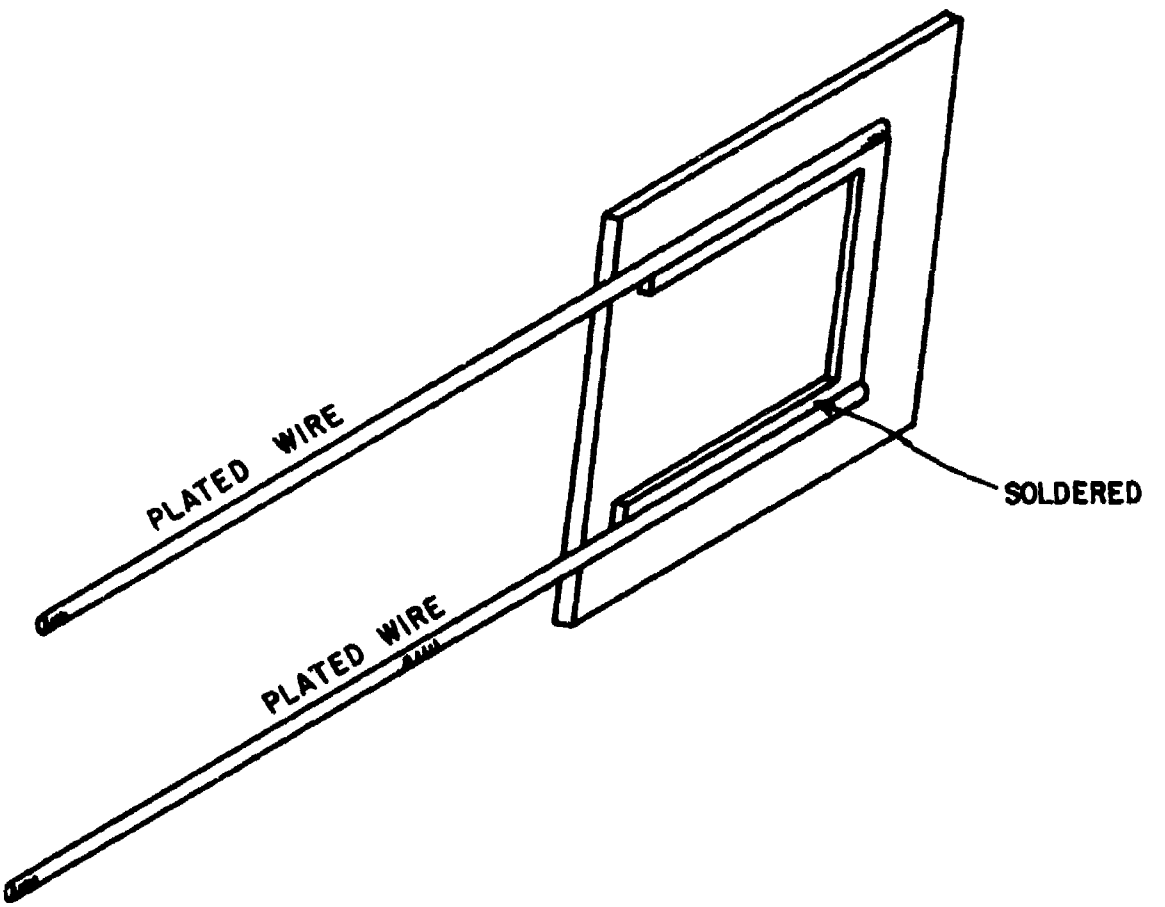


Figure 12. UNIVAC Printed Circuit Hairpin

In setting up a plane, the spacing of the plates wires is a problem to be considered. Interaction does exist between neighboring wires. If a plated wire is placed 15 mils away from a test wire, the current required to drive the test wire will increase approximately 11 percent (in the absence of keepers) because of the demagnetizing field from the neighbor. Figure 13 shows some approximate interactions as more wires are added in a simple no-keeper geometry. It should be obvious, however, that a keeper design can temper the sensitivity shown. However, since for a realistic density typical center-to-center spacing between plated-wire configurations lies in the range of less than 12.5 mils, other configurations have been considered to minimize such reactions between the wires.

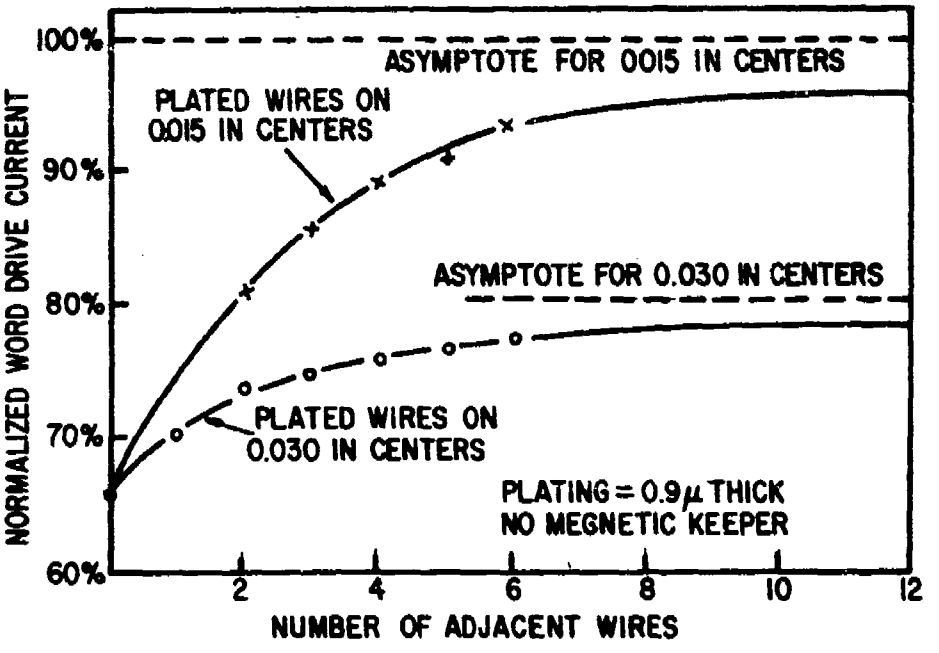


Figure 13. Normalized Word Drive Current Increase Caused by Adjacent Wires

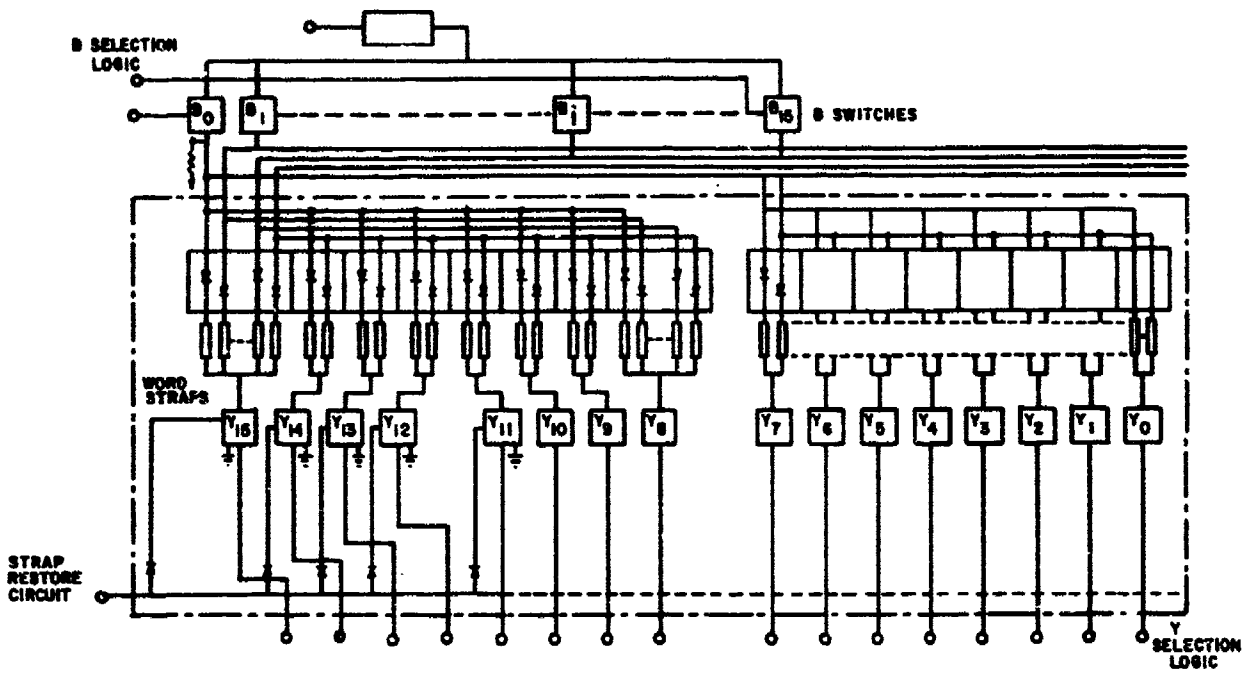
On highly specialized memories, addressing circuits can be designed so that adjacent wires are not called. This has no practicality for random access memories. The standard procedure, therefore, has become two interweave dummy wires that may be plated or not plated, grounded or floating to pick up the

stray noise and memory plane edge effects to reduce the noise levels. No information is currently established to estimate an optimum ratio of the dummy wires in the array to the "live" wires, but both Honeywell, Inc. and UNIVAC use one dummy wire for every six live ones in some systems.

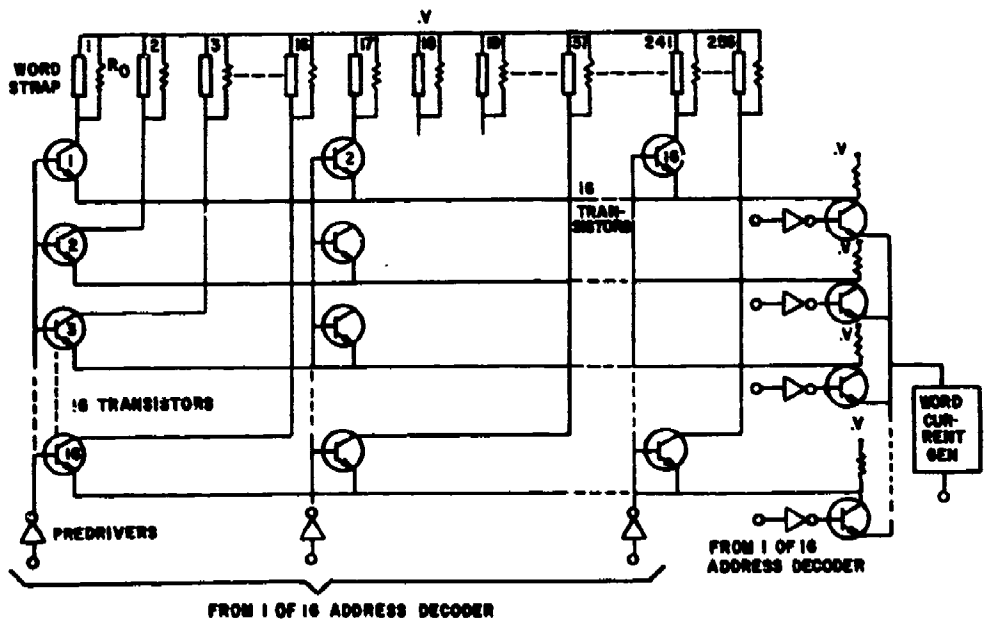
This report has, so far, emphasized 5-mil systems. This is because most published information is based on this system, these systems are currently operational, and the properties of other size wires can be compared generally on an extrapolated basis, if necessary. Discussion with current manufacturers indicate that 2-mil plated wire, called by the trade name Miniwire, is the way new memory designs are to be based. Its advantages far outweigh its faults. The Miniwire easily permits wire-to-wire spacing of 10 mils and bit spacing along the wire of 25 mils. On top of this, the effective use of such low 25-ma bit currents and 250-ma word currents (compared to 100 ma and 850 ma) make it completely compatible with medium scale integrated (MSI) and large scale integrated (LSI) circuits.

The Miniwire word electronics allows a single selection transistor per word strap organized for base and emitter matrixing. The conventional selection technique in 5-mil systems consists of a number of diodes connected to a common switch rail. Transistor drive circuits have long been recognized, for reasons shown below, to be superior to diode railing. However, if individual transistors were used, the cost would be prohibitive, and the currents needed to drive 5-mil circuits are too large for integrated circuit internal transistor compatibility. The railing together of the diode word straps shown in figure 14a permits undesirable currents to flow in unselected word straps. Not only do these currents introduce partial readouts into the system, but they require additional circuitry to restore capacitance charge associated with a half-selected rail when operated at higher speeds. With the use of transistor selection, only the specific word strap selected is connected to the current source. The other straps remain at constant potential.

The selection and subsequent interrogation of this single word strap eliminates the need for a capacitance stack restore helping produce a quieter system. By using this method, the total system reliability is greatly enhanced, packaging complexity is reduced, and power requirements are lowered.



a. Typical Diode Selection Matrix



b. Word Selection Electronics (256-word plane)

Figure 14. Selection Circuits

SECTION III

MEMORY ORGANIZATION AND OPERATION

The electronics needed to control the plated-wire memory operation are not unlike similar electronics needed to control ferrite core memories. The problems, besides the accuracy of timing, of course, are not so much in the concept complexity of the electronics, but in the large count of components needed to do the job. The development, thereby, is aimed at getting MSI and LSI circuits in as many spots as technically feasible to reduce the volume and number of components to be handled in producing the memory.

Specific circuits vary considerably from system to system even though the concepts are basically the same. So this section will present the electronics from a system concept approach and, when the situation demands, focus in on a sample circuit. As long as the reader understands that the samples may be not related to each other, and that they may be theoretical circuits, extendable to a system in-hand, no confusion should result.

The circuits to be considered are addressing circuits, circuits that control and read bit current through the plated wire, and circuits that control current to the word straps. Clock and sensing circuits are necessary for operation but are generally governed as part of the interface with peripheral sensors, and so will not be emphasized here.

The consideration of addressing circuits is important in the sense that a large volume of the plated-wire system is made up of the addressing electronic components. The circuits to be considered must be balanced against each other in the speed of address access, operation reliability, lack of crosstalk, and minimum number of components. Many times these factors are mutually competing. One representation to the addressing concept can be seen in figure 15. To reference one of the 256 intersections in the array (i.e., one core space), four switches or flags must be set. First, choosing an X-drive and an X-sink uniquely selects one of the 16 X-lines. The diodes prevent secondary current paths. Next, choosing a Y-drive and Y-sink flag in conjunction with this isolates the address member of the core. The darkened lines in the figure intersect at address X31, Y23.

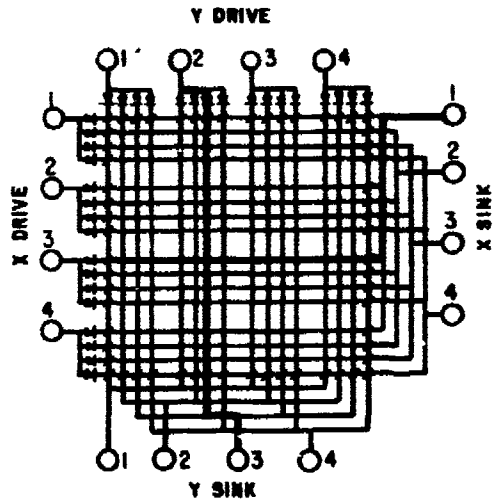


Figure 15. Addressing Concept Model

This concept can be expanded to the plated wire directly or with variations. One variation is shown in figure 16, a simple system concept in which a two-wire plated element is terminated in a differential sense amplifier. Its use in the plated-wire UNIVAC 9000 series commercial 36,864 bit memory has carried the addressing to an economic minimum. As can be seen from this figure, plated wires, instead of terminating directly in a differential amplifier-digit driver arrangement, terminate in a 9 x 16-matrix switch box that connects nine sense amplifier-digit drivers to 16 sense-bit (plated-wire) lines. Each switch routes the proper signals from the plated wires to the sense amplifiers, and routes the bit currents from the bit drivers to the proper wires.

When a word is read from the memory, 16 words of nine bits each are stimulated to generate sense signals. Each of the nine sense amplifiers is connected through the matrix of switches to one of the possible 16 bits. The correct connection is determined by the decoded address. Thus, only sense signals from the desired wire are amplified at the memory-processor interface as data; the other 15 words that generated sense signals are ignored. Since the readout is nondestructive, ignoring these signals does not affect the data.

On the other hand, when new information is written into a single word, the word strap selects 16 words, in any of which the bit write current could change the stored information. But the unique matrix connects each bit driver to a sense bit line so that only one new word is written.

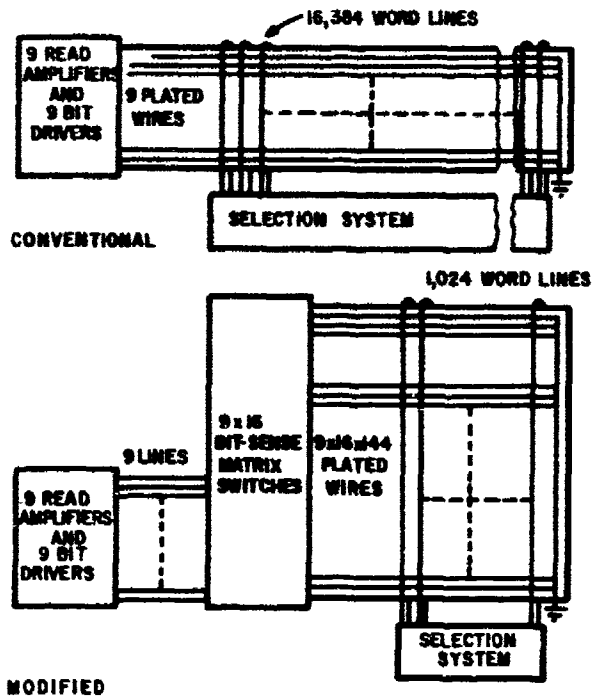


Figure 16. UNIVAC 9000-Series Addressing Model

It should be noted that this operation is possible only if the word-current amplitude for writing is no larger than word current used for NDRO. Otherwise, the other 15 words would face potential destruction.

This organization has a much higher address decoding efficiency than most other magnetic film memories, and it is an economical way of reducing the number of word lines. It approximates 3D organization. But, unfortunately, the electronic interaction in the matrix switch and the close tolerance needed in controlling word-current make it impractical to attempt hardening in a radiation environment, and, hence, its use is limited in military systems.

Therefore, more straightforward approaches such as the basic digit selection and the base-emitter coupling procedures as illustrated in section II are generally implemented.

To drive current in the plated wire, three sense-digit drive configurations will be described: a single-ended direct-coupled, a single-ended transformer-coupled, and a balanced transformer-coupled. These drive configurations are shown, respectively, in figures 17, 18, and 19. The driver circuitry is on the

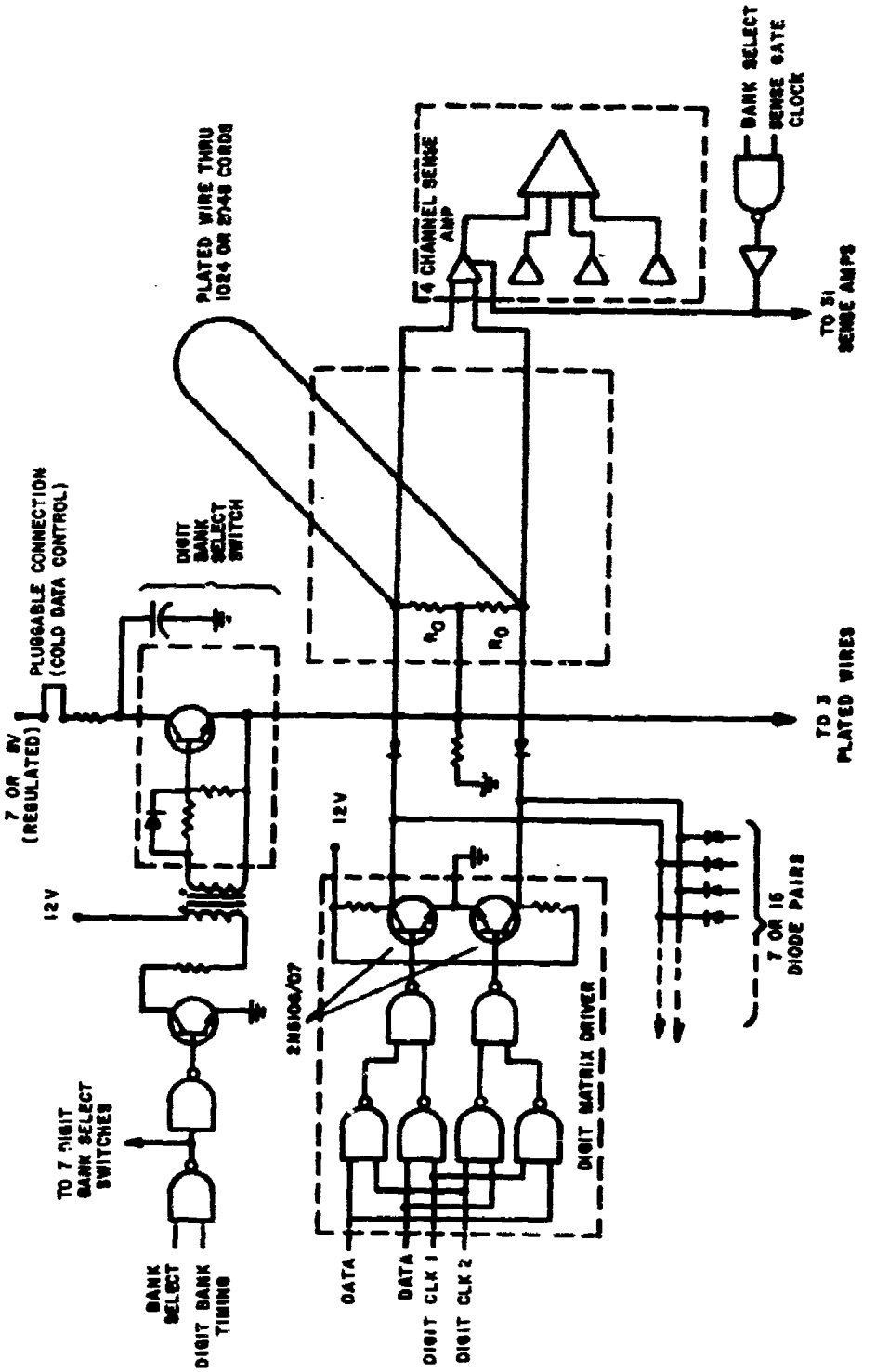


Figure 17. Single-Ended, Direct-Coupled Drive/Sense Electronics

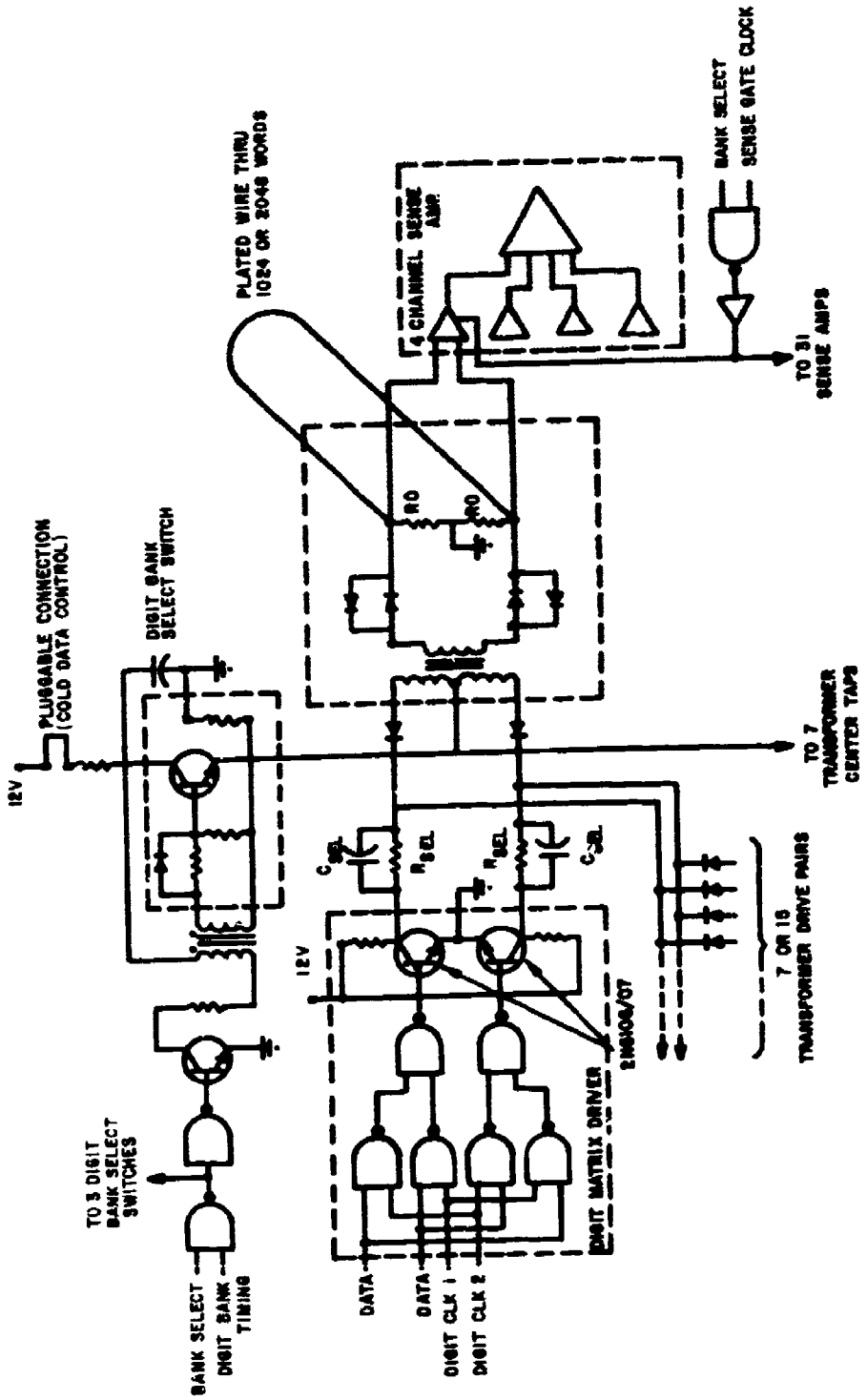


Figure 18. Single-Ended Transformer-Coupled Drive/Sense Electronics

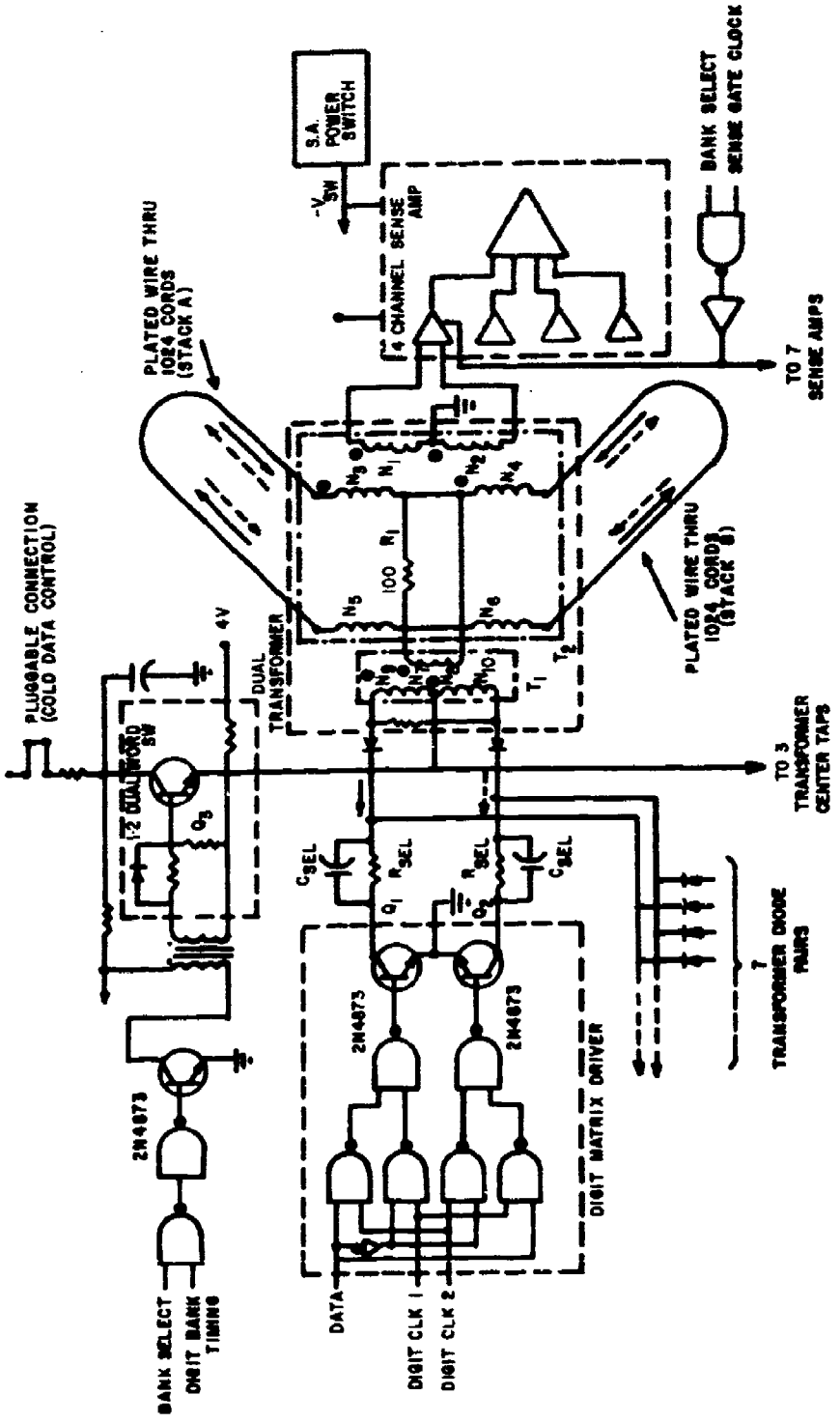


Figure 19. Balanced Transformer-Coupled Drive/Sense Electronics

left of the plated wire and the sensing circuitry is on the right. You will note that coming into the transistor base from the digit matrix driver are two clock pulses, one with the data and the other with the complement of the data. As was mentioned in the last section, repetitious writing of the same bit at the same bit address will cause a magnetization "creep" of the adjacent bits. That is, bits adjacent to the bit being written will shift in amplitude and direction. However, by first writing the complement and then the data, no more than two repetitious signals will ever be written at the same location.

The difference between the single-ended configurations and the balanced configurations lies in the terminating network connections at the input to the sense amplifiers. If one plated-wire pair is connected to the terminating network it is a single-ended drive; if two plated-wire pairs are connected, it is a balanced drive. Of the three configurations shown the power consumed in writing is least in the single-ended, transformer-coupled circuit and is declared by Honeywell as having the lowest technical risk of the three in production. The single-ended, direct-coupled configuration consumes the most power in its writing and is the most vulnerable of the three to radiation. The balanced method requires significantly less packaging space, and, on a comparative basis, rates best in standby power consumption, reliability, and performance during radiation exposure.

Like the three drive/sense configurations for plated-wire drive, three configurations can also be shown for word strap drive: transistor-per-word drive, direct-coupled drive, and transformer-coupled drive. These are illustrated, respectively, in figures 20, 21, and 22. The transistor-per-word drive has the least consumption of standby and write power of the three configurations considered. Its reliability is not quite as high, however, and its radiation vulnerability is high. Thus, while it is still a good circuit for commercial uses it would be more advantageous to turn to other circuits for military use.

The smallest physical size can be found in the direct-coupled configuration. This is sometimes a major consideration in the determination of military and space systems. Many times, according to Honeywell Aerospace engineers, military systems designers define physical dimensions for a subsystem, i.e., a memory stack, and then contract out to build a memory of specified electrical characteristics that will fit the physical space allotted. The direct-coupled

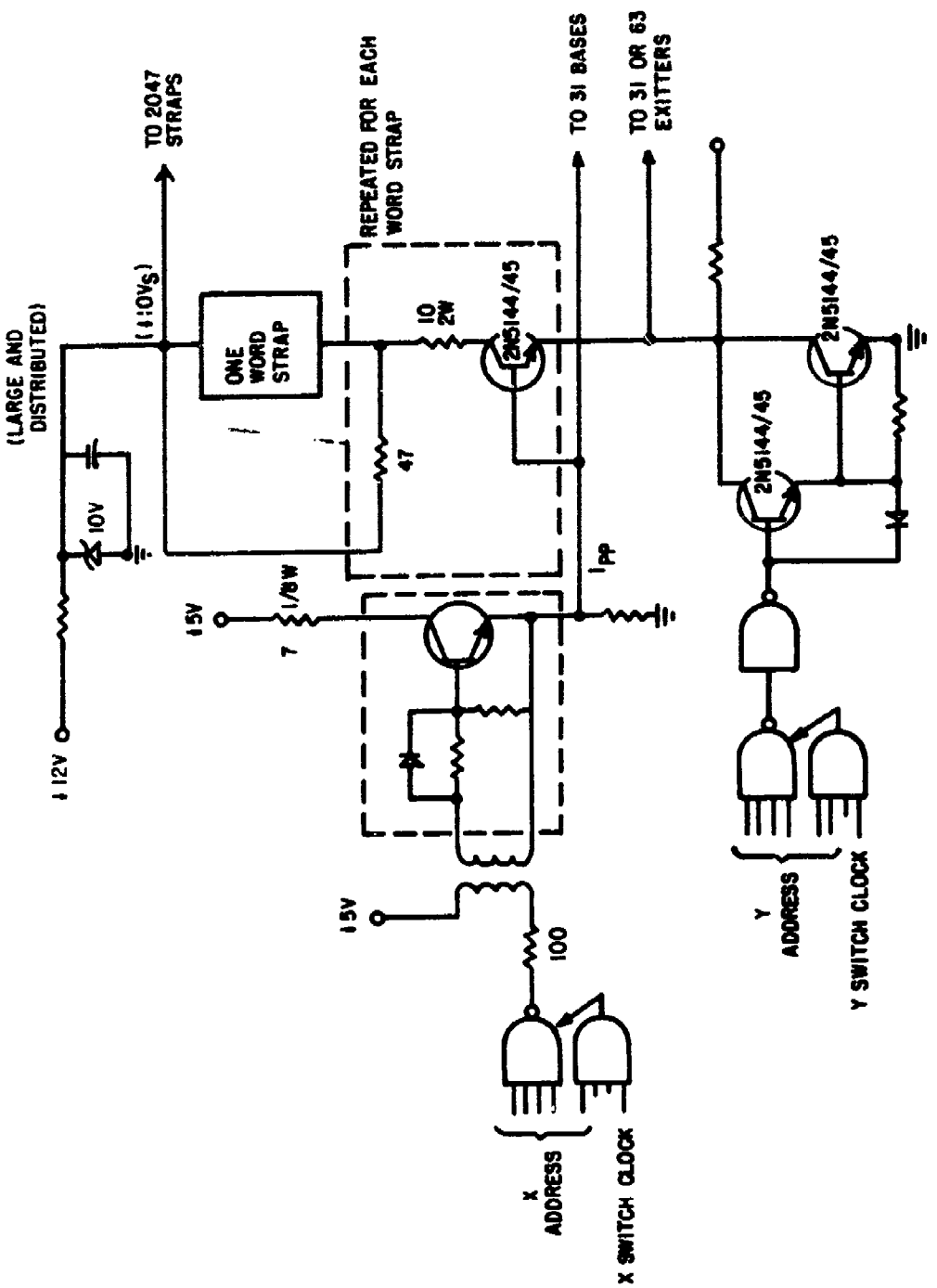


Figure 20. Transistor-per-Word Drive Electronics

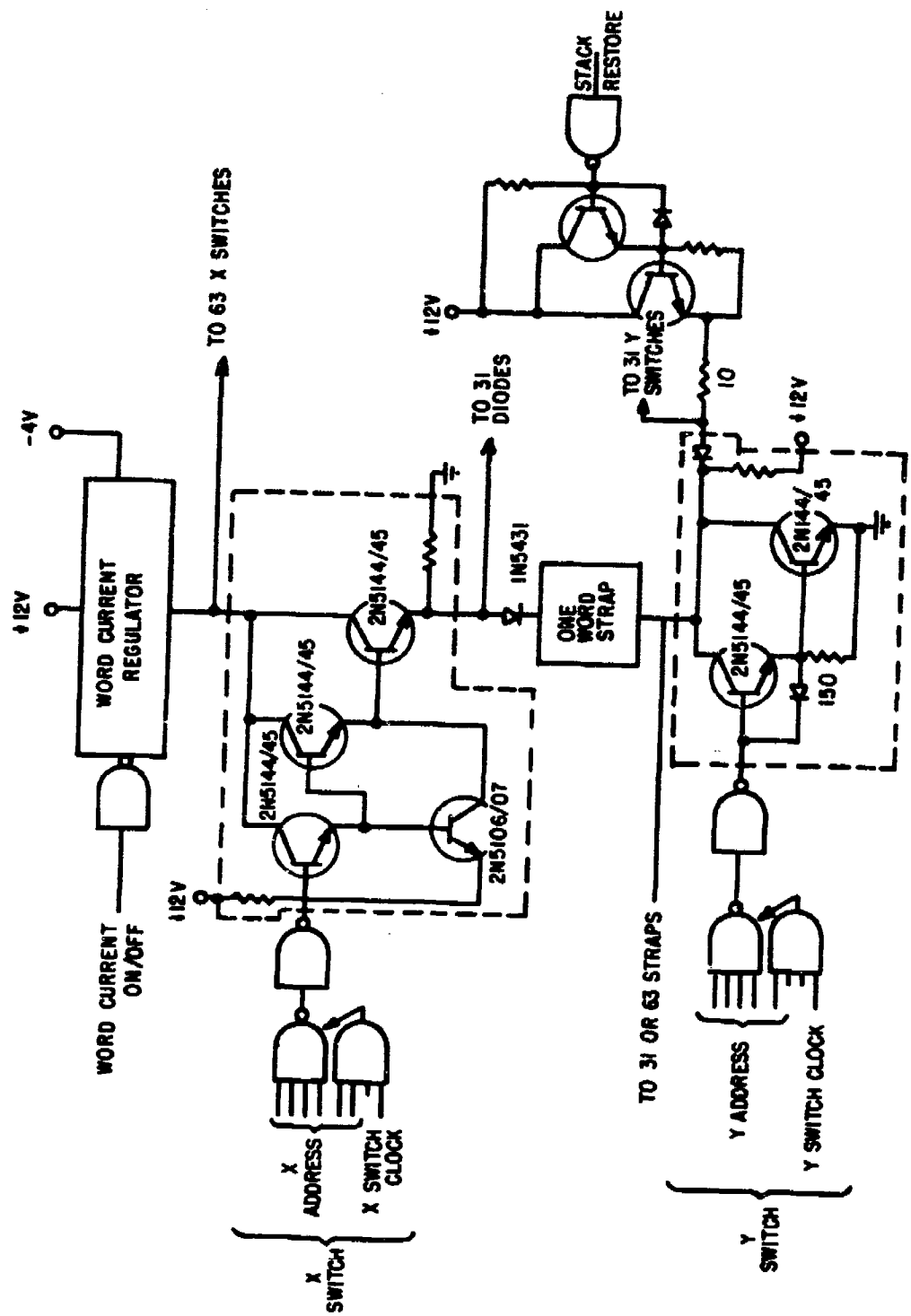


Figure 21. Direct-Coupled with Diode Matrix Word Drive Electronics

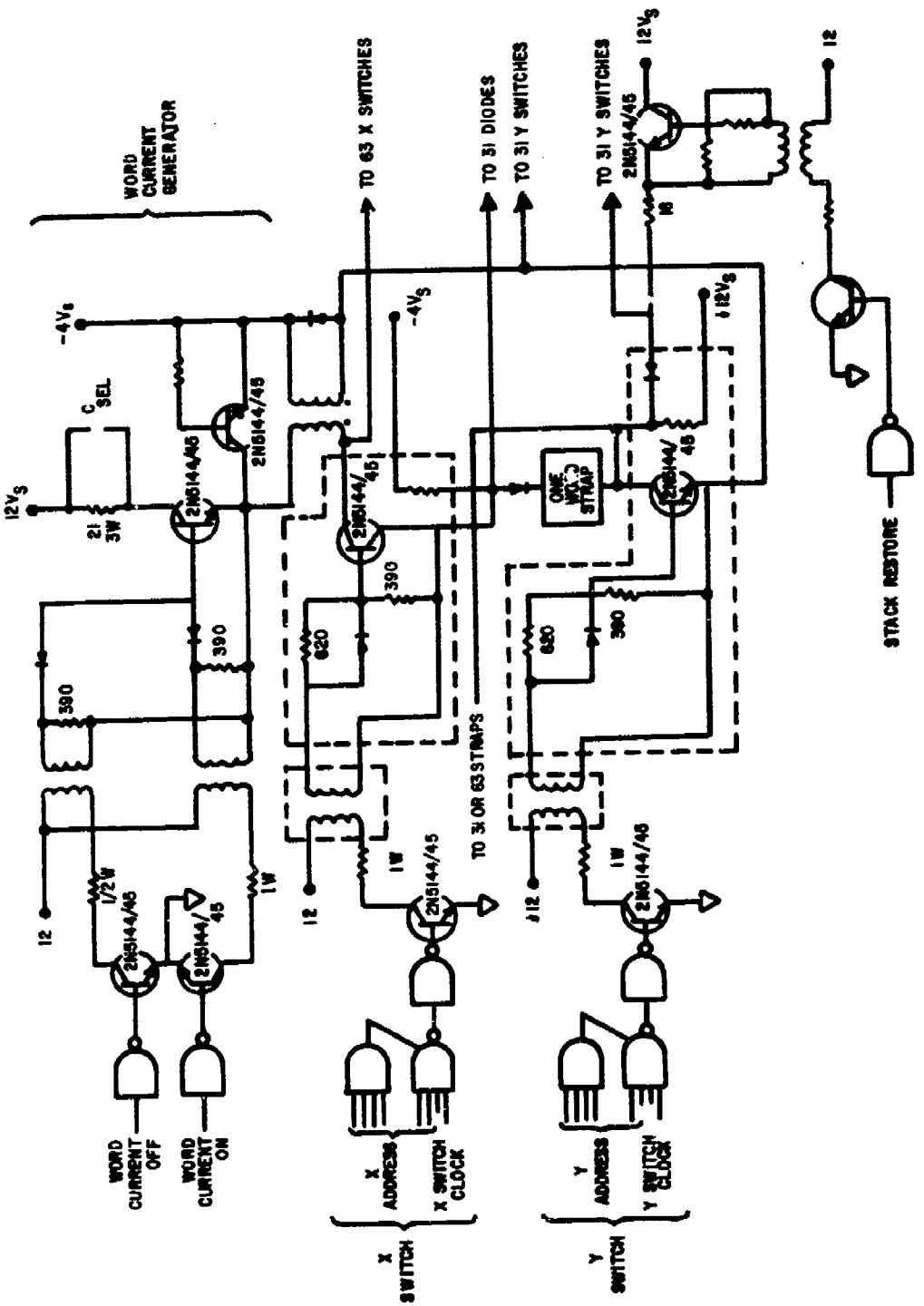


Figure 22. Transformer-Coupled with Diode Matrix Word Drive Electronics

configuration's other characteristics are comparable to the transformer-coupled approach, but the latter does have the best isolation in a radiation environment and the highest reliability of the three.

The concepts presented above probabily will not change much when new circuits are designed, but since 2-mil Miniwire is coming into predominance, the currents needed to drive it become less by one or two orders of magnitude. While the circuits above are basically discrete component circuitry, the low-current requirements permit them to be extended easily to IC and hybrid circuitry.

Additional concepts are also designed into the above circuits to prevent current surges, improve reliability, increase hardness, etc., but these will not be discussed here. The circuits must be evaluated each on an individual basis according to the design criteria. In military systems. particular emphasis must be placed on preventing the scrambling of data stored in the memory in the presence of gamma-induced transients. A current "circumvention level" is generally defined such that transient currents above this criterion are shunted to bypass circuitry. The contents of a particular location being written during the transient might be lost, but other memory locations will retain their data in spite of the malfunctioning interface signals. Care should be taken in the design of the word drive circuits. In general a coincidence of word and bit digit currents are needed to alter a bit, but a heavy overdrive of word current alone, generally in excess of 150 percent, can destroy a bit. Circuits should not be overly dependent on transistor h_{fe} because neutron bombardment causes degradation of this parameter.

While the examples used here are for a single stack of plates wires, hardened systems should consist of twin stacks of plates wires sharing a common set of digit/sense electronics through transformer coupling networks; this tends to balance out radiation-induced signals. Floating grounds and transformer isolation further reduce transient noise problems.

SECTION IV

POTENTIAL VULNERABILITY OF PWM TO NUCLEAR RADIATION

One of the basic functions of the Air Force Weapons Laboratory (AFWL) is to ensure hardness of military systems to nuclear radiation. Some of the radiation problems have been mentioned in this report, but this section will focus attention on this problem.

Gulf Radiation Technology has made a radiation study of the plated-wire element. In this section we will summarize its results and finish with a discussion of the associated electronics.

Magnetic materials have been subjected to various radiation burst environments at simulators and at underground tests in the last few years to determine vulnerability levels. These tests have included displacement effects studies of the magnetic material exposed to neutron and electron fluences, and studies of the response of devices to electron, γ-, or X-ray pulses, transient magnetic fields, and mechanical stress or shock. On the whole, magnetic materials used in magnetic memories have been very hard to displacement effects. In general, neutron fluences in excess of 10^{16} n/cm^2 (E > 10 keV) are required for perceptible change in the magnetic properties of typical magnetic materials. This is several orders of magnitude above vulnerability threshold of semiconductor devices.

When a significant amount of energy is absorbed in a material in a time which is short compared to the materials acoustic relaxation time, a thermomechanical shock can be generated. It is known that strong mechanical shock can reverse magnetic fields and, in a memory, can cause amnesia. Permalloy, in a theoretical sense, has a designed zero-magnetostriction coefficient, and as such, it should not be susceptible to mechanical shock. In practice, however, there is some susceptibility, but it is at least an order of magnitude less than that experienced by ferrite cores. Gulf Radiation Technology has found that this susceptibility is increased, however, when the mechanical effect is imposed synergistically with other effects. The degree of susceptibility is discussed in the classified report GULF-RT-A11060, Radiation Effects on Magnetic Devices.

The energy deposition in magnetic devices can destroy the magnetic characterization of such a device if the resulting temperature rise exceeds the Curie temperature. The Curie temperature for plated wires is in the 500° to 600°C range. Typical ferrite cores have Curie temperatures of 150°C to 250°C, so the plated wire is much less temperature sensitive than the cores.

The hardening of associated electronics is a technology that is fairly well developed at the present time. First of all, the system should be hardened against photocurrent (I_{pp}) generation. In the word strap circuits these extraneous currents can cause erroneous readouts, as can interface noise voltages and other interface current surges. Therefore, the design should use semiconductor devices having small minority carrier collecting volume. A good hardened circuit design minimizes the number of semiconductors by the use of pulse transformers. Circuits can be hardened by the use of low-impedance paths, the use of I_{pp} compensation, the use of balanced circuits, current limiting, shunting, and clamping techniques.

A prompt ionizing dose of radiation can cause enhanced conductivity in dielectrics that can result in damaging current surges. This effect can be minimized by making a careful choice of capacitor types and by using adequate IC metalization thickness. The circuit configuration should allow for capacitor ionization discharge effect and use sufficient resistances for current limiting. Balanced organization, transformer isolation and careful selection of materials aid also.

Device types that degrade under total ionizing dose should be eliminated whenever possible.

Semiconductor devices used should have shallow junctions, narrow base regions, be heavily doped, and possibly be gold doped to maximize h_{fe} and reduce h_{fe} variation into a neutron environment. The circuit should use feedback techniques and use a minimum number of semiconductors.

The casing should be a heavy shield with maximum case integrity to minimize electromagnetic pulse (EMP) effects.

SECTION V

CONCLUSION

No attempt has been made in this report to show the superiority or weakness of the plated-wire memory to other forms of memories that may be used. This report is tutorial, not an evaluation report. Sometimes, however, comparisons put the figures in proper perspective and greatly aid understanding.

As far as vulnerability to radiation effects is concerned, magnetic cores are intrinsically harder than semiconductor memories, and because of the zero-magnetostriction coefficient designed into the plated-wire memory, and the non-destructive readout capability, the PWM is harder than ferrite cores. The switching speeds of PWM, which are far superior to the iron cores, switch in 1/16 the time, dissipating only 1/11 of the switching energy. The plated thin film memory is faster and uses less switching energy than the plated wire, but the output voltage of the film is only 10 percent of the plated wire which makes it highly vulnerable to noise. On the other hand, the ratio of the plated-wire output signal to the ferrite core is about 1/4 which, in this respect, places it at a similar disadvantage.

The plated-wire memories and the semiconductor have similar switching speeds, but the semiconductor does have a slight edge. The disadvantage of semiconductor memories is its vulnerability to radiation environments.

Ferrite cores generate heat in switching and require a heat sink; for the plated wire, no measurable heat is generated.

In satellites, low-power consumption is a most basic design factor. Plated wires excel here. In an experimental setup, UNIVAC ran a 100-k bit memory continuously in a 100-kHz serial mode (ideal operation) and consumed only 0.3 watt. More realistic usage generally equals about 3 to 10 watts which is still less than the minimum 20 watts needed to run a comparable ferrite core.

APPENDIX

TWO-DIMENSIONAL, TWO-AND-ONE-HALF DIMENSIONAL, AND THREE-DIMENSIONAL WORD SELECTION PRINCIPLES

Straight selection schemes to select a byte (a group of bits that may or may not define a word) in a memory core storage requires about two diodes for every byte selected. For any practical memory this becomes an inordinately large number. For example, one 16-bit decoder for a 65,536 byte memory requires 132,228 diodes. The impracticality of this for larger memories is obvious, and so, other selection schemes have been devised. Their analogical resemblance to geometrical configurations has given them the descriptive names of two-dimensional (2D), two-and-one-half dimensional (2-1/2D), and three-dimensional (3D) schemes.

In a 2D configuration the storage elements are organized so that identification of an element is done by referencing separate X- and separate Y-drive lines--each of which is determined by half of the address bits--oriented in a single plane. In the schematic shown in figure 23, a vertical Y-line represents a word line; the horizontal X-line, the bit line, that intersects the Y-lines defines the storage core spaces. W drivers are needed in this setup to reference W words, but this is not impractical since economical word drivers are available. The economy also increases as the word lengths (the number of bits per word) get larger, as long as the total words plus bits stay constant. To get this, memory designers like to define an "aspect ratio," k, a factor by which the number of bits in 2D is increased and the number of words decreased. For this design, the values of k are less than or equal to the square root of W divided by the square root of B, the number of bits.

The 2-1/2D scheme is a variation of the 2D system, but, as will be seen, does have aspects of the 3D system. The k in this case is best large. The plane is set up so kB lines lie in the bit direction and W/k lines lie in the W direction. To select a word, a single word line and kB bit lines are half-selected. Some of these kB bit lines are simultaneously working by feeding bit drivers and other sense amplifiers through B decoder circuits. Determination of the wanted signal is determined by each of these decoder circuits having the capability of 1/k selection. The selection of a bit is faster, but not as economical as the 2D system.

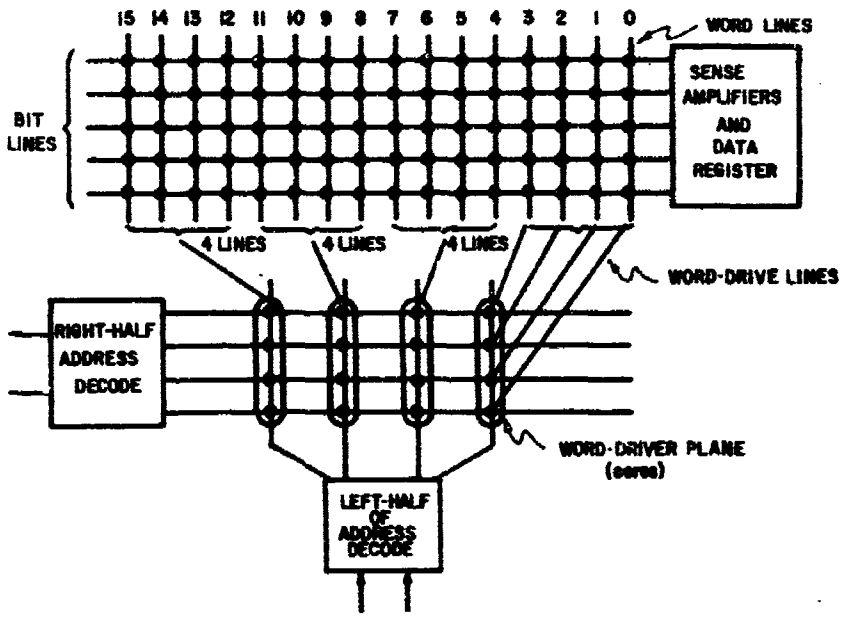


Figure 23. Two-Dimensional Organization of Memory

Unique selection out of several signals is done in the 3D setup by use of an extra winding. The memory configuration consists of a stacked array of B memory planes, each of which contains W storage spaces, so that a single plane contains 1 bit of all words. The X-line is equivalent to the word line contained within one plane. The Y-line interacts between planes. The extra winding, the "Z" or "inhibit" winding, is added interacting between the planes, and set up, physically perpendicular to both X- and Y-drive axes. This is considered the most efficient of the three configurations but has the drawback of operation only in the destructive readout capability, which capability is not generally considered an asset to plated-wire operation.

Write operation in the 3D mode is done in a two-step cycle. First, the selected word bits are initially zeroed; then, the attempt is made to change these zeros to ones. The Z-winding, however, is programmed to inhibit--hence, the name--the writing of certain of these bits, depositing in the memory the word to be written. This is a fast process for two-cycle write operations and needs only 2W drivers.

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13. ABSTRACT

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A wire plated with a magnetic surface can be used as a computer memory element by alternating the polarity of the magnetic field. While the wire in different enclosure configurations can hold its field in either a longitudinal or a radial direction, the radially oriented field currently is found to have many advantages with respect to switching speed, radiation hardness, and associated peripheral equipment. The construction of the wire presents many parameter balancing problems and needs very tight environmental controls for practical production. These problems have not yet been eliminated, keeping the bit cost in these memories high. The performance, however, of the radially oriented type compared to ferrite cores and semiconductor memories augments this high cost. A recently developed 2-mil wire size element eliminates some of the problems found in the previously standard 5-mil wire systems.

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